WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 75
ARBITRARY
WAVEFORM GENERATOR

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

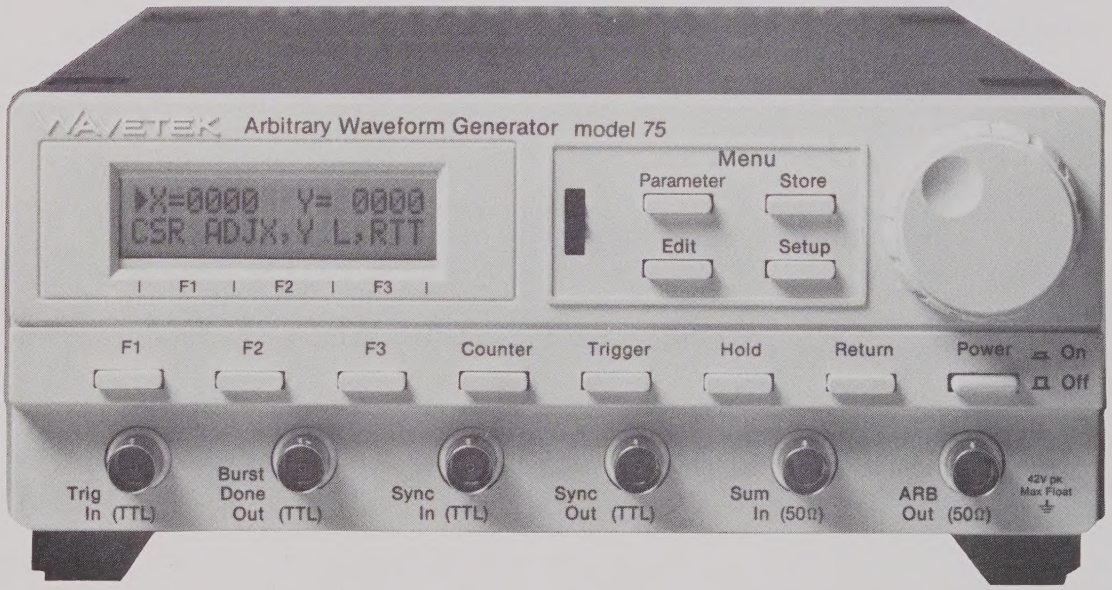
The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.

WARNING

This equipment uses a BR-2/3A, 3V lithium battery, that contains less than 0.5 grams of lithium. To prevent the release of a potentially harmful substance, ***DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE BATTERY****. In addition, observe correct polarity when replacing.*



Model 75 Arbitrary Waveform Generator

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 75

The Model 75 is a versatile, yet easy to use arbitrary waveform generator. It contains advanced waveform editing features that allow the user to easily create and edit complex waveforms.

1.2 WAVEFORM EDITING

The editing features are based on a pair of points called "thumbtacks". These thumbtacks are placed at each end of the portion of the waveform to be edited, then the appropriate editing feature is invoked. The thumbtacks will appear as bright dots on an oscilloscope using Z-axis modulation.

1.2.1 Standard Waveforms

Standard waveforms are inserted between the thumbtacks. A standard waveform can be the entire waveform or only part of it. The standard waveforms are sine, cosine, inverse sine, haversine (inverse cosine), triangle, square, ramp up, ramp down, and dc. These standard waveforms can then be edited using the other editing features if desired.

1.2.2 Rubber Band Editing

Rubber band editing is analogous to stretching a rubber band between two thumbtacks. A cursor is placed between the thumbtacks which can be moved in either the X or the Y direction. The waveform is then stretched from each thumbtack to the cursor in real time.

1.2.3 Digital Amplitude and Digital Offset

The section of the waveform that is between the thumbtacks can be adjusted in amplitude and offset in real time without affecting the rest of the waveform.

1.2.4 Point Edit

Individual points of the waveform can also be adjusted in real time.

1.3 STANDARD FEATURES

1.3.1 8192 × 4095 Point Waveform Resolution

The waveforms have a vertical resolution of 4095 points and a horizontal resolution adjustable from 2 to 8192 points. The waveform memory is broken up into four blocks of 2048 horizontal points. This can be used as one waveform of up to 8192 points or as four different waveforms (one active and three stored) of up to 2048 points each.

1.3.2 Crystal Controlled Frequency

The waveform clock (sample frequency) is crystal controlled and adjustable from 20 mHz to 2 MHz (500 ns to 50 s), allowing a waveform period of 1 μs to 113.8 hours. The frequency is adjustable as either waveform frequency, waveform period, or sample frequency. An external TTL level clock of up to 2 MHz can also be used as the waveform clock (sample freq).

1.3.3 Operating Modes

The Model 75 can operate in continuous, triggered, gated, toggled, or burst modes. All modes except continuous are initiated (triggered) by either a front panel pushbutton or an external signal. In these modes the waveform stops at break points which can be inserted anywhere in the waveform (by default one breakpoint will be at the start address), then waits for another trigger. In burst mode, a predetermined number of waveforms (from 1 to 1,048,575) is generated before stopping.

1.3.4 Internal Waveform Counter

In gated, toggled, and burst modes an internal counter can be used to display the number of complete waveforms since the last trigger. This is particularly useful for monitoring a burst of waveforms or counting the number of waveforms for fatigue testing.

1.3.5 Hold Function

A front panel pushbutton or external signal will cause the waveform to stop at the current output level and remain there until the hold is released.

1.3.6 Return Function

A front panel pushbutton or external signal will cause the output to ramp back to the start value. The rate of this ramp is adjustable from 0 (instant return to start) to 100 ms per vertical point.

1.3.7 Stored Waveforms

Three additional waveforms may be stored (with their parameter settings) in waveform memory. These may later be recalled into, or exchanged with the active waveform. This feature is only available with horizontal resolutions of 2048 points or less.

1.3.8 Nonvolatile Instrument Setup

The complete instrument setup is stored in battery backed up memory so that it will not have to be reset after the power has been turned off.

1.3.9 Series Operation

Several Model 75's can be connected in series, each one producing a burst of waveforms, with their outputs summed together (using the "sum in" connector). This can be used to produce long waveforms or unusual sequences such as 50 "normal" waveforms and then 1 "abnormal" waveform.

1.3.10 Parallel Operation

Several Model 75's can be connected in parallel to create phase coherent arbitrary waveforms. The phase relationship is completely adjustable with a resolution equal to the horizontal resolution of the waveform. This feature is useful in three axis mechanical testing and multi-phase power applications.

1.3.11 Communications Options

Either an IEEE-488 or RS-232-C communication interface is available to transfer waveform data and control the Model 75 from a computer.

1.4 SPECIFICATIONS

1.4.1 Standard Waveforms

DC, square, triangle, up-ramp, down-ramp, sine, cosine, inverse sine, and haversine waveforms are provided. Each of these waveforms can be stored into the waveform memory between thumbtacks automatically, and then edited with the waveform editing functions if desired.

1.4.2 Operational Modes

Continuous
Output runs repetitively from the programmed start address to the programmed stop address.

Triggered
Output quiescent until triggered by external signal or front panel pushbutton, then runs until another break point is encountered. Break points can be inserted anywhere in the waveform with the default break point at the beginning of the waveform.

Gated
Same as triggered mode except that the output is continuous for the duration of the gate signal and until the first break point encountered after the gate signal ends.

Burst
Same as in the triggered mode except that a programmable number of waveforms is counted before the waveforms stop. The maximum burst is 1,048,575 waveforms.

Toggled
The output is quiescent until triggered. It then runs continuously until another trigger stops the waveform at the next break point.

1.4.3 Waveform Resolution

Normal Waveform
2048 points horizontal × 4095 points vertical.

Chained Waveform
8192 points horizontal × 4095 points vertical. Stored waveforms are not available with chained operation.

1.4.4 Sample Rate

Range
0.02 Hz to 2.0 MHz (50 s to 500 ns)

Waveform Period and Frequency
The actual waveform period is the number of horizontal points (from start to stop address) times the sample time. This can range from 1 microsecond for a square wave to 113.8 hours for a waveform using all 8192 points.

Frequency Resolution
4 digits

Frequency Accuracy
± 0.015%

Repeatability (24 Hr)
± 25 ppm

Temperature Coefficient
≤5 ppm/°C

1.4.5 Output Signals

Amplitude

Range: ± 0.005 to 5 Vp into 50Ω (0.01 to 10 Vp-p into 50Ω). ± 0.01 to 10 Vp into an open circuit (0.02 to 20 Vp-p into an open circuit).

Resolution: 3 digits.

Accuracy: ± 1.8% of setting and ± 2.5 mV for amplitude + offset ≥0.5V.
± 1.8% of setting and ± 0.25 mV for 0.5V > amplitude + offset ≥50 mV.
± 1.8% of setting and ± 25 μV for 50 mV > amplitude + offset.

Repeatability (24 Hr): ± 0.1% of setting.

Temperature Coefficient: ≤150 ppm/°C of setting.

Offset

Range: + 5V to − 5V into 50Ω (− 10V to + 10V into an open circuit). Absolute amplitude plus offset may not exceed ± 5V into 50Ω (± 10V into an open circuit).

Resolution: 3 digits.

Accuracy: 2% of setting and ± 15 mV for amplitude + offset ≥0.5V.
2% of setting and ± 1.5 mV for 0.5V > amplitude + offset ≥50 mV.
2% of setting and ± 0.15 mV for 50 mV > amplitude + offset.

Repeatability (24 Hr): ± 5 mV and ± 0.1% of setting.

Temperature Coefficient: ≤(± 1 mV ± 150 ppm)/°C of setting.

1.4.6 Outputs

ARB Out (50Ω)

Source of primary waveform output. Maximum amplitude is ± 5 Vp into 50Ω. Output is fuse protected.

Sync Out (TTL)

Will drive up to 10 LSTTL loads. This is a pulse 1 sample time wide that is usually used to sync an oscilloscope or another ARB generator. Pulse position is adjustable to any point in the waveform.

Burst Done Out (TTL)

Will drive up to 10 LSTTL loads. A TTL low indicates that the waveform is running. TTL high indicates that the instrument is waiting for a trigger in triggered, gated, toggle, or burst modes. Used primarily to start another ARB generator in series operation.

Ref Out (TTL)

Will drive up to 10 LSTTL loads. This pulse train at the sample frequency is used primarily as a reference source for other ARB generators in series operation or in parallel operation.

Z-Axis Out

This signal is a pulse, adjustable in amplitude from 2 to 14 volts, that is used to modulate the Z-axis of an oscilloscope when using the waveform editing features. The logic polarity is also selectable.

1.4.7 Inputs

Sum In (50Ω)

The signal at this input is added to the arbitrary waveform to produce an output (at waveform out) of the sum of the two. A peak input of ± 5V will produce an output equal to the amplitude setting. Input is fuse protected. Accuracy is 4% (2% if internal fuse is shorted).

Trig In (TTL)

Impedance is 100 KΩ. Signal is used to control the generator in the trigger, gate, toggle, and burst modes. Slope polarity is selectable.

Sync In (TTL)

Impedance is 100 KΩ. A high input causes the waveform to restart at the start address. Primarily used for synchronizing several arbitrary waveform generators in parallel operation.

Ref In (TTL)

Impedance is 100 KΩ. This signal input is used for the sample clock when the external ref is selected.

Hold In

Impedance is 100 KΩ. A TTL low or switch closure at this input causes the generator to stop at the current output level and remain there until released by a TTL high or switch opening.

Return In

Impedance is 100 KΩ. A TTL low or switch closure at this input causes the output level to ramp back to the start value. The ramp rate is front panel selectable from 0 to 100 ms per point.

1.4.8 Trigger Sources

Manual

Use the Trigger pushbutton switch on front panel to operate internal trigger circuitry. The slope polarity can be set via the display menus.

External

Use the communication ports (GPIB or RS-232-C) or the Trig In connector on front panel. Trig In connector frequency input can be up to 1 MHz. The slope polarity can be set via the display menus.

1.4.9 Waveform Characteristics

Horizontal Resolution
Up to 8192 points.

Vertical Resolution
4095 bits (−2047 to +2047).

Rise/Fall Time
<350 ns.

1.4.10 Communication Ports (Optional)

IEEE-488 Port (Option 001)
Type: IEEE-488-1978 compatible, non-isolated, double buffered.

Address: 0-30, internal DIP switch selectable or front panel selectable.

Subsets: SH1, AH1, T6, TE0, L4, SR1, RL1, PP0, DC1, C0, E1.

RS-232-C Serial Port (Option 002)
Communication is full duplex (bi-directional) with CTS/DTR or XON/XOFF handshaking.

Connector: Rear panel mounted DB-25 (female) with DCE or DTE configuration.

Data Format: 8 bits, no parity, one stop bit.

Data Rate: 14 steps internal switch selectable (50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19,200).

1.4.11 General

Environmental
Temperature Range: +23°C ±5°C for specified operation, operates 0 to +50°C, −20 to +75°C for storage.

Warmup Time: 20 minutes for specified (guaranteed for 1 year) operation.

Vibration: 5 to 55 Hz with maximum of 2g at 55 Hz.

Shock: 30g, 11 ms half sine.

Altitude: Sea level to 10,000 ft. for operation. Sea level to 40,000 ft. for storage.

Relative Humidity: 95% at 25°C and at sea level (non-condensing).

Dimensions: 21 cm (8.27 in.) wide, 10 cm (3.94 in.) high, 32.3 cm (12.72 in.) deep.

Weight: 3.55 kg (7.8 lb) net, 4.68 kg (10.3 lb) shipping.

Power: 90 to 128, 180 to 256 rms; 48 to 66 Hz; 1 phase; <25 VA.

1.4.12 Options

001: IEEE-488 (GPIB) Port
For instrument control or entering waveform data.

002: RS-232-C Serial Port
For instrument control or entering waveform data.

NOTE

Options 001 and 002 are mutually exclusive.

SECTION 2
INITIAL PREPARATION

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of three terminals, the earth ground terminal is the non-matching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Line Voltage

Refer to table 2-1 to determine the proper selection of the line voltage connector. Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 3/8 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit and a 3/16 amp fuse installed.

2.2.2 Verifying the Line Voltage

To verify the line voltage (or change the fuse), the operator must first remove the top and bottom covers. Remove the top and bottom using the following steps and figure 2-1.

1. Remove two (2) screws holding top and bottom covers to rear panel.
2. Slide both covers (together as a unit) to the rear and remove from the chassis assembly.

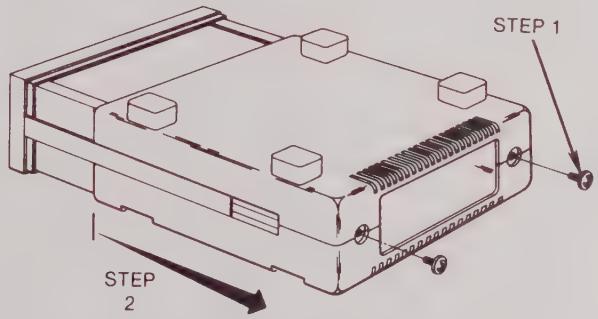


Figure 2-1. Top and Bottom Cover Removal

After the covers have been removed, the line voltage can be checked by viewing the voltage label through the inspection hole as shown in figure 2-2.

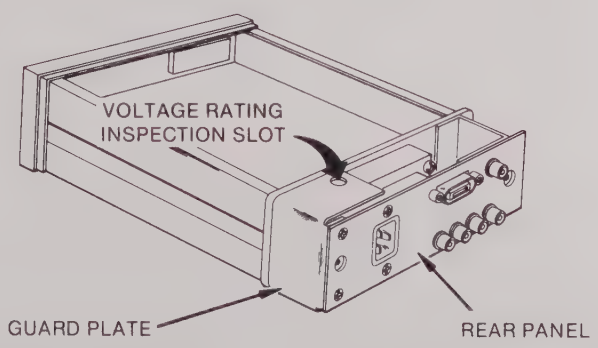


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct according to table 2-1, perform the following steps and refer to figure 2-3 for steps 1 and 2, and figure 2-4 for steps 3 thru 6 to change the line voltage and fuse.

1. Remove the two screws holding guard plate to the rear panel.
2. Remove the guard plate from the rear panel.

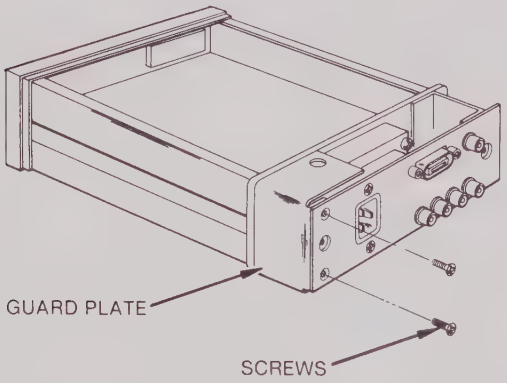


Figure 2-3. Guard Plate Removal

3. Remove the voltage selector connector from the ac primary board. Rotate the connector until the correct voltage selector indicator is on top.
4. Reinstall the voltage selector connector.
5. Remove the fuse and install new fuse as called out in table 2-1.

Connector Position	Voltage Range	Fuse
115V	90 to 128 Vac	3/8 amp
220V	180 to 256 Vac	3/16 amp

Table 2-1. Voltage/Fuse Selection

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the guard plate is attached to the unit.

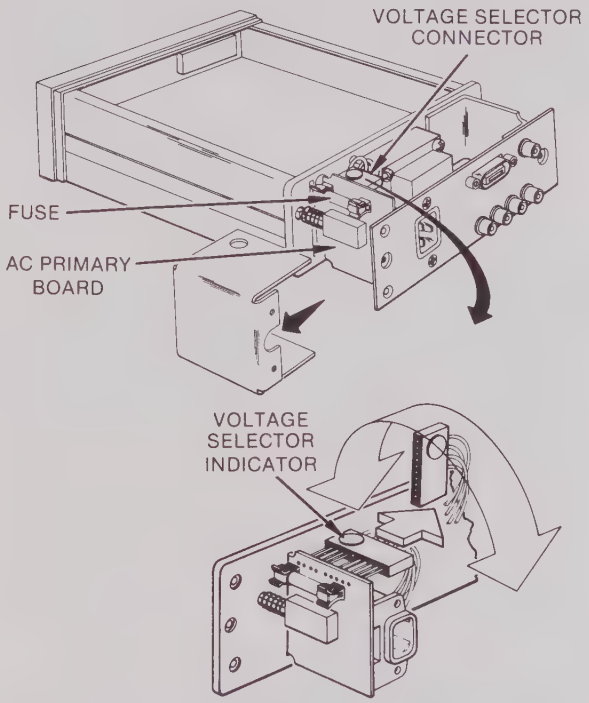


Figure 2-4. Fuse and Voltage Selection

Reassembly

Refer to figure 2-5 for step 1 and figure 2-6 for steps 2 thru 5.

1. Insert the guard plate over the ac primary board and voltage selector connector and align with screw holes in the rear panel. Secure with two screws.

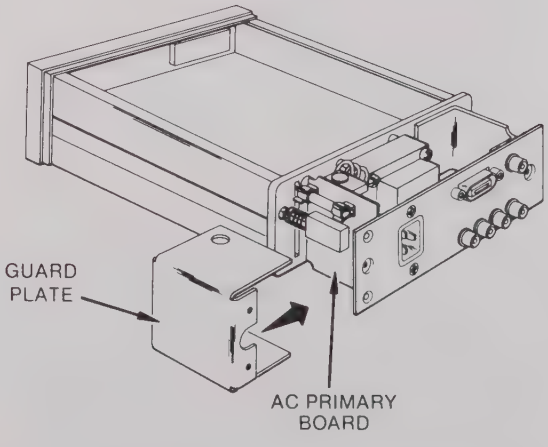


Figure 2-5. Rear Chassis Assembly

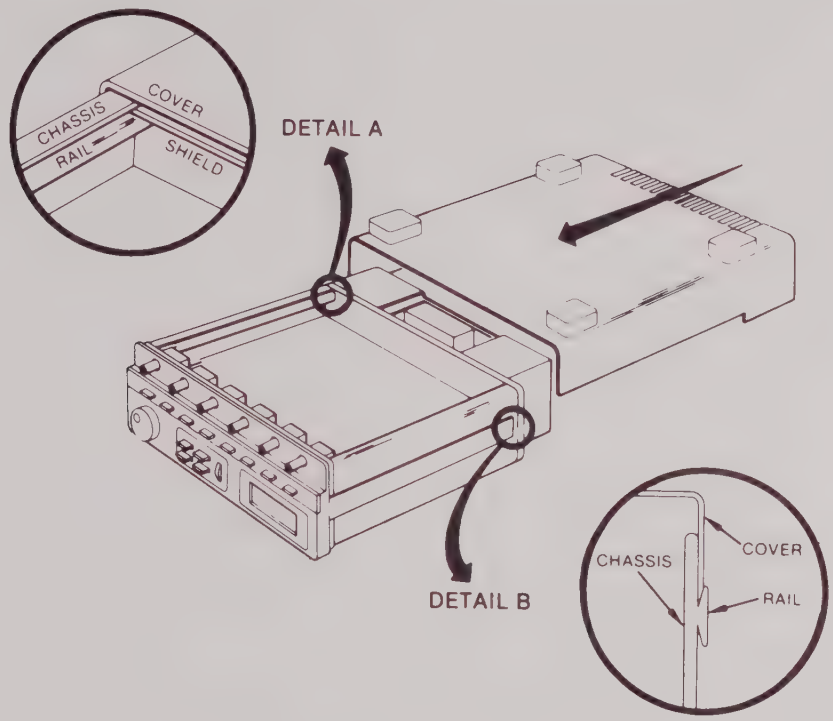


Figure 2-6. Top and Bottom Cover Installation

2. Turn the instrument upside down, position the bottom cover over the guard shield and rear panel. Slide the bottom cover forward approximately two (2) inches while engaging the top cover shield slides (see figure 2-6, detail A) and the outside slide rails (see figure 2-6, detail B).
3. Turn the instrument right side up. Install the top cover using the same procedure as in step 2.
4. Align the rear of both the top and bottom cover with each each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly together and slide the chassis assembly into top and bottom covers.

CAUTION

When sliding on the bottom cover, avoid moving the ribbon cables located near the power transformer.

5. Secure covers to unit using two screws as shown in figure 2-1.

2.2.4 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

NOTE

Signal ground may be floated up to ± 42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.2.5 Interface Connections

The GPIB (Option 001) I/O rear panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

NOTE

The terms "GPIB" and "IEEE-488" are used synonymously in this manual.

2.2.6 GPIB Address

For Option 001 instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB default address can be changed by resetting the internal DIP switch (for access, remove the top cover, see paragraphs 2.2.2 and 2.2.3) or changed temporarily by pressing the front panel ADRS soft key and rotating the Control knob when the GPIB address is displayed.

The switch sections are labeled from 1 thru 5 and their OPEN position noted (OPEN = Binary "0" in table 2-2). To verify the address, press ADRS soft key on the front panel.

Table 2-2. GPIB Address Code

Device	Listen	Talk	1	2	3	4	5	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	1	0	0	0	0	21	41
2	"	B	0	1	0	0	0	22	42
3	#	C	1	1	0	0	0	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	1	0	1	0	0	25	45
6	&	F	0	1	1	0	0	26	46
7	'	G	1	1	1	0	0	27	47
8	(	H	0	0	0	1	0	28	48
9	)	I	1	0	0	1	0	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	1	1	0	1	0	2B	4B
12	,	L	0	0	1	1	0	2C	4C
13	-	M	1	0	1	1	0	2D	4D
14	.	N	0	1	1	1	0	2E	4E
15	/	O	1	1	1	1	0	2F	4F
16	0	P	0	0	0	0	1	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	0	1	0	0	1	32	52
19	3	S	1	1	0	0	1	33	53
20	4	T	0	0	1	0	1	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	0	1	1	0	1	36	56
23	7	W	1	1	1	0	1	37	57
24	8	X	0	0	0	1	1	38	58
25	9	Y	1	0	0	1	1	39	59
26	:	Z	0	1	0	1	1	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	0	0	1	1	1	3C	5C
29	=	]	1	0	1	1	1	3D	5D
30	>		0	1	1	1	1	3E	5E

NOTE: Address 31 is not allowed

2.2.7 The RS-232-C Connectors

The RS-232-C I/O rear panel pin connections and signal names are given in table 2-3. The panel connector is a DB-25 female connector (see figure 2-7) and will connect to a standard RS-232-C cable (interface type E). The data format is an 8-bit, no parity, one stop bit. The baud rate is selectable from those listed in table 2-5 using dip switch S1 (figure 2-8).

Table 2-3. RS-232-C Data In/Out

Pin	Name	Direction (DCE Configuration)	Direction (DTE Configuration)
2	TXD[1]	IN	OUT
3	RXD[2]	OUT	IN
4	RTS[3]	N/C	OUT
5	CTS[4]	OUT	IN
6	DSR[5]	OUT	IN
7	SIG GRD	—	—
8	RLSD[6]	OUT	IN
20	DTR[7]	IN	OUT

(Remaining Pins Not Connected)

[1]Transmit Data
[2]Receive Data
[3]Request to Send
[4]Clear to Send
[5]Data Set Ready
[6]Receive Line Signal Detect
[7]Data Terminal Ready

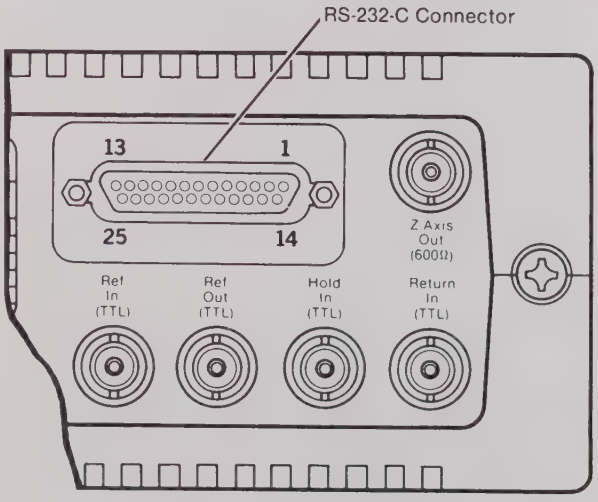


Figure 2-7. RS-232-C Connector Pinouts

The following is a description of pin functions. Actual installation is covered in paragraph 2.2.8.

In the DCE configuration, pins 2 and 3 are data input and output respectively and must be used. Pin 5 may be used to indicate that the Model 75 is ready to receive data. Pin 20 tells the Model 75 that the connected device is ready to receive data, but may be connected to pin 6 of the Model 75 if the other device is always ready. Pin 7 is signal ground and must be used. Pins 6 and 8 will be positive (asserted) when the Model 75 is on.

In the DTE configuration, pins 2 and 3 are data output and input respectively and must be used. Pin 4 will be positive whenever the Model 75 is On. Pin 5 tells the Model 75 that the connected device is ready to receive data. If the other device is always ready, pins 4 and 5 of the Model 75 may be connected together. Pins 6 and 8 are properly terminated inputs but have no function. Pin 20 will be positive when the Model 75 is ready to receive data. Pin 7 is signal ground and must be used.

The handshaking method is front panel selectable as CTS/DTR (hardware) or XON/XOFF (see paragraph 3-32 for more information).

2.2.8 Connecting the RS-232-C Interface

Before connecting the Model 75 using the RS-232-C interface, the correct configuration (DCE or DTE) must be selected and the internal ribbon cable connected to either the DCE or DTE location (see figure 2-8) on the RS-232-C option board. To determine which configuration is correct, you will need the manual for the device to which you are connecting the Model 75. The following assumes that the other device has a DB-25, RS-232-C connector.

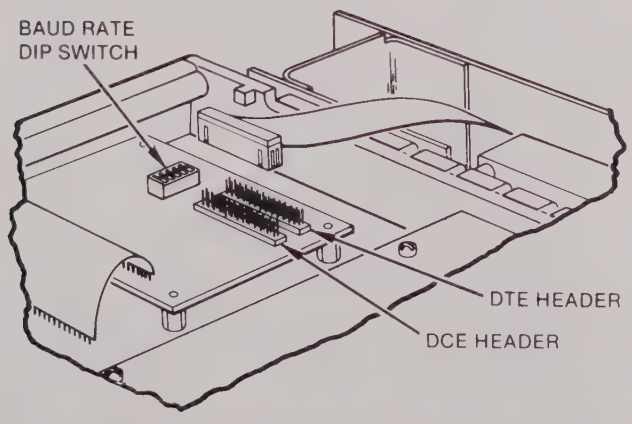


Figure 2-8. Baud Rate Switch and DTE/DCE Connections

1. Determine if the other device is a DCE device or a DTE device. If this is not explicitly spelled out you will need to look at the pin out for its connector. If pin 2 is the data output, the device is a DTE (most computers). If pin 3 is the data output, the device is a DCE (most modems). Configure the Model 75 as the opposite type of device by connecting the internal option cable to the appropriate header (see figure 2-8).

2. In most cases a straight through cable can be used to connect the Model 75 with the other device. The Model 75 only requires the connection of pins 2, 3, 5, 7, and 20 but the other device may require more. Examples of typical cable assemblies are shown in figure 2-9. However, there are many interpretations of the RS-232-C standard and either of the following procedures (a or b) should be used to ensure that the control and handshake signals are properly connected.

   a. If the Model 75 is configured as a DCE then;

      (1) Pin 7 (signal ground) is always connected straight through.

      (2) Pins 2 and 3 are connected straight through if DCE/DTE configuration is correct.

      (3) Pin 5 of the Model 75 will need to be connected to an input of the other device that will enable and disable the character transmission from that device. If the other device does not support this, XON/XOFF handshaking will be required and pin 5 can be left disconnected.

      (4) Pin 20 of the Model 75 should be connected to an output pin on the other device that indicates when it is ready to accept data. If the other device does not have such a pin but is not always ready, it can send XOFFs and XONs to indicate readiness. When using this method, or if the other device is always ready to accept data, this pin can be connected to an always positive pin on the other device or to pin 6 or 8 on the Model 75.

      (5) Pins 6 and 8 are always positive when the power is on and can be connected to any pins on the other device that require being held positive.

   b. If the Model 75 is configured as a DTE then;

      (1) Pin 7 (signal ground) is always connected straight through.

      (2) Pins 2 and 3 are connected straight through if DCE/DTE configuration is correct.

(3) Pin 20 of the Model 75 will need to be connected to an input of the other device that will enable (positive) and disable (negative) the character transmission from that device. If the other device does not support this, XON/XOFF handshaking will be required and pin 20 can be left disconnected.

(4) Pin 5 of the Model 75 should be connected to an output pin on the other device that indicates whether or not it is ready to accept data. If the other device does not have such a pin but is not always ready, it can send XOFFs and XONs to indicate readiness. When using this method, or if the other device is always ready to accept data, this

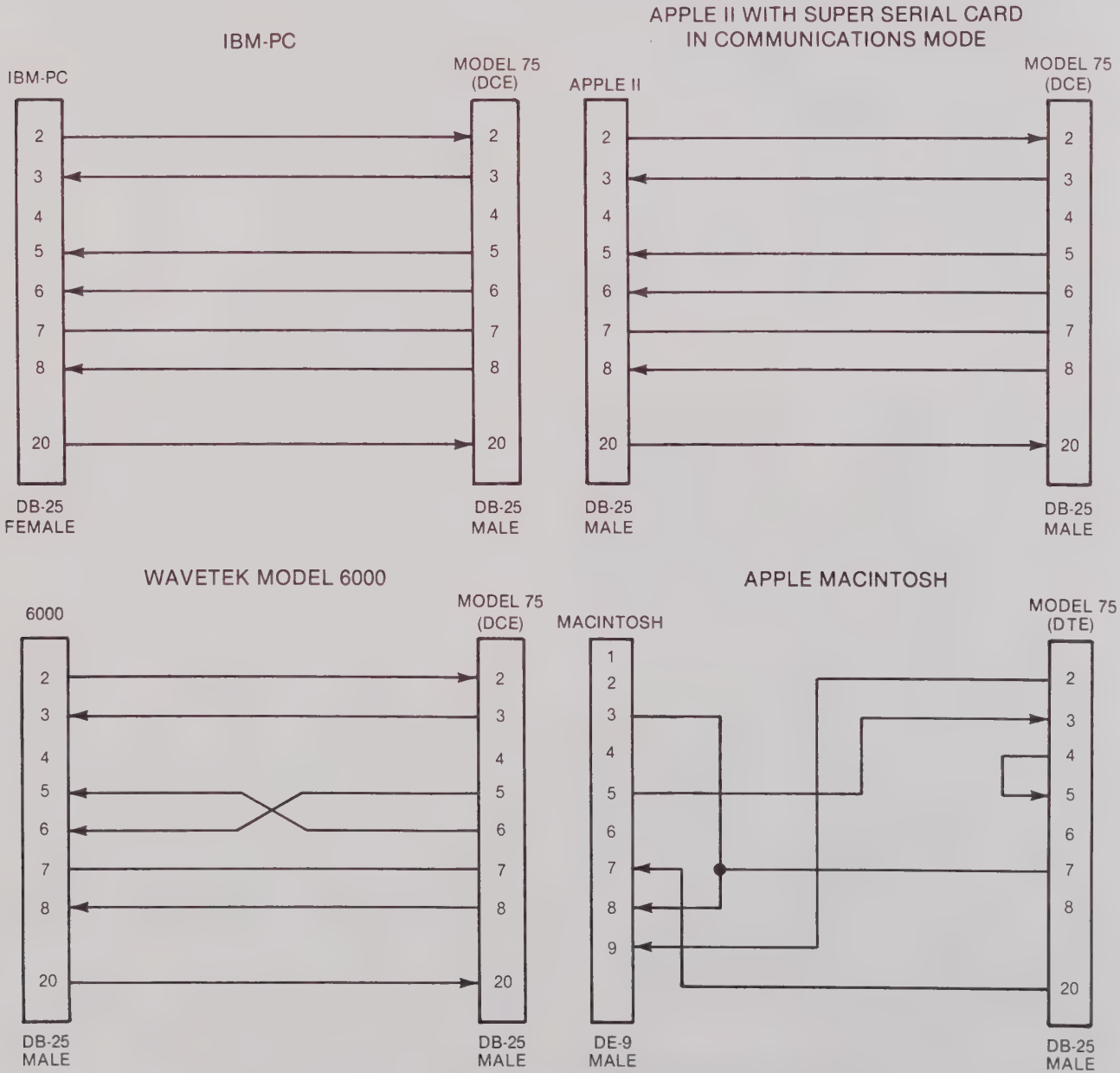


Figure 2-9. Typical Examples of Serial Cables

pin can be connected to an always positive pin on the other device or to pin 4 on the Model 75.

(5) Pin 4 is always positive when the power is on and can be connected to any pin on the other device that requires being held positive.

(6) Pins 6 and 8 are properly terminated inputs but have no function.

NOTE

Any pins not mentioned in the previous list are not connected in the Model 75 and therefore can be connected to anything if the connections are already present in the cable.

3. The handshaking method is front panel selectable as CTS/DTR (hardware) or XON/XOFF (see paragraph 3.31 for more information).
4. Set the baud rate on the Model 75 to the highest rate that is available on both the Model 75 and the other device by setting the dip switches (figure 2-8) according to table 2-4.
5. Configure the other device for the same baud rate as in step 4, 1 stop bit, 8 data bits, and no parity.

Table 2-4. RS-232-C DIP Switch Settings

Baud Rate	SW1-4	SW1-3	SW1-2	SW1-1
19,200	Closed	Closed	Closed	Open
9,600*	Open	Closed	Closed	Closed
4,800	Open	Closed	Closed	Open
2,400	Closed	Open	Open	Open
1,800	Open	Closed	Open	Closed
1,200	Open	Closed	Open	Open
600	Closed	Open	Open	Closed
300	Open	Open	Closed	Open
200	Closed	Open	Closed	Open
150	Open	Open	Open	Closed
134.5	Closed	Open	Closed	Closed
110	Open	Open	Open	Open
75	Closed	Closed	Open	Open
50	Closed	Closed	Open	Closed

*This is the factory set position

NOTE 1. SW1-5 should always be OPEN

2. Factory connector configuration is DCE

2.3 INITIAL CHECKOUT PROCEDURE

The Model 75 ARB waveform generator will supply a variety of waveforms at the ARB Out connector that can be modified at will using the front panel controls. In order to verify the operation of the controls and the functions/modes/values that they control, the generator must first be set up to produce an output and then the effect of the controls on the output and the display indications noted. While this procedure verifies functional operation of this instrument, it does not verify the calibration. The values shown are typical values and should only be used as a guide. Required tools and test equipment are shown in table 2-5.

Table 2-5. Test Equipment and Tools

Instrument	Comments
Oscilloscope*	Dual channel, 20 MHz min. bandwidth with external trigger and Z-axis capability.
50Ω Feedthrough	2% accuracy, 2W
BNC Tee	1 male to 2 female
BNC Coax Cable	RG58U, ~ 3 ft. length (4 each)
Signal Source**	1 MHz capability with square wave (10 Vp-p into 50Ω) and TTL output.
Frequency Counter	Capable of both frequency and period measurements.

*Check the oscilloscope manual to determine the maximum allowable Z-axis input voltage. Do not exceed that voltage.

**A second Model 75 can be used as the signal source. For the TTL signal requirements, use the Ref Out connector on the rear panel and use the SAMPL soft key to set the frequency. For the 1 kHz, 10 Vp-p signal, use the STOP soft key to set the stop address to 1999, use the FREQ soft key to set the frequency, and use the FUNC and EXEC soft keys to select a square wave. See section 3 for more detail.

To verify the overall operation of the Model 75 ARB waveform generator, follow the procedure in table 2-6. Refer to the referenced figures and tables for appropriate test equipment connections and settings. Refer to figure 3-1 and paragraph 3.2 for control and connector locations.

Table 2-6. Checkout Procedure

Step	Control/Switch	Position/Operation	Observation/Comments
1	Power	Press On	Display indicates "WAVETEK MODEL 75". Adjust the LCD viewing control for best contrast.
This step verifies the "Reset" functions of the Model 75.			
2	Setup	Press three times	
	F2 (Reset)	Press once	Display indicates "RESET Ver x.xx".
	F3 (Exec)	Press once	Display indicates "RESET Ver x.xx X".
This step verifies the "Z-Axis" functions of the Model 75.			
3	Setup	Press once	Connect the Model 75 as shown in figure 2-10. Set equipment controls as indicated in table 2-7.
	F2 (ZLOGIC)	Press once	Display indicates "ZLOGIC NEG" or "ZLOGIC POS".
	Control knob	Rotate until display indicates "ZLOGIC POS".	Oscilloscope will indicate a dc level of 0 Vdc ±1V with positive-going pulses.
	Control knob	Rotate until display indicates "ZLOGIC NEG".	Oscilloscope will indicate a dc level of 2, 4, 6, 8, 10, 12, or 14 Vdc with negative-going pulses.
	F1 (ZLEVL)	Press once	
	Control knob	Rotate CW until display indicates "ZLEVEL 14V".	Oscilloscope will indicate a dc level of +14V ±1V with negative-going pulses.
	Control knob	Rotate CCW to step display through the selectable settings.	Oscilloscope will indicate the selected voltage ±1V with negative-going pulses. Leave Setting at "ZLEVEL 2V".
This step sets the "Z-Axis Out" voltage level and polarity.			
4			Connect the Model 75 as shown in figure 2-11. Set equipment controls as indicated in table 2-8.
	Control knob	Rotate CW or CCW to set acceptable contrast between trace and thumbtacks. Adjust oscilloscope intensity if required.	If thumbtack intensity is too bright at +2V, terminate the Z-axis cable with a 50Ω load. If the thumbtacks are dimmed instead of intensified, set ZLOGIC to POS.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
This step verifies the "Waveform Memory" functions of the Model 75.			
5	Store	Press two times	Reset the oscilloscope horizontal sweep to 1 ms/DIV.
	F2 (CHAIN)	Press once	
	Control knob	Rotate until display indicates "CHAIN 8K".	
	F3 (EXEC)	Press once	
	Edit	Press two times	
	F1 (FUNC)	Press once	
	Control knob	Rotate until display indicates "FUNC SINE"	
	F3 (EXEC)	Press once	Oscilloscope will indicate slightly more than one cycle of the sine wave at approximately 10 Vp-p.
	Edit	Press two times	
	F1 (START)	Press once	Display will indicate ">ST = 0000 SP = 8191".
	Control knob	Rotate CW	Oscilloscope waveform start point will move from left to right until waveform disappears. Display will now indicate ">ST = 8191 SP = 8191".
	Control knob	Rotate CCW	Oscilloscope waveform start point will move from right to left until waveform is complete. Display will now indicate ">ST = 0000 SP = 8191".
	F2 (STOP)	Press once	Display will indicate "ST = 0000 >SP = 8191.
	Control knob	Rotate CCW	Oscilloscope waveform stop point will move from right to left until the waveform disappears. The display will now indicate "ST = 0000 >SP = 0000".
	Control knob	Rotate CW	Oscilloscope waveform stop point will move from left to right until the waveform is complete. The display will now indicate "ST = 0000 >SP = 8191".
	Store	Press two times	
	F2 (CHAIN)	Press once	Display indicates "CHAIN 8K".
	Control knob	Rotate until display indicates "CHAIN 2K".	
	F3 (EXEC)	Press once	
	Edit	Press two times	
	F1 (FUNC)	Press once	Display indicates "FUNC SINE".
			Set the oscilloscope sweep to .5 ms/DIV.
	F3 (EXEC)	Press once	Display will indicate "FUNC SINE X". Oscilloscope will display less than 3 cycles of a sine wave of approximately 10 Vp-p.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
	This step verifies the "Amplitude Control" functions of the Model 75.		
6	Parameter	Press two times	
	F1 (AMPL)	Press once	Display will indicate "AMPL 5.000 Vp".
	Control knob	Rotate CCW	Oscilloscope amplitude decreases smoothly to minimum of approximately 10 mVp-p. Display will now indicate "AMPL 5.00 mVp".
	This step verifies the "Offset" functions of the Model 75.		
7	F2 (OFFSET)	Press once	Display will indicate "OFFSET 0.0 mV".
			Reset oscilloscope vertical gain to 2V/DIV.
	Control knob	Rotate CW	Oscilloscope will increase smoothly to approximately 5.10V. The display will now indicate "OFFSET 5.10V".
	Control knob	Rotate CCW	Oscilloscope level decreases smoothly to approximately −5.10V. Display will now indicate "OFFSET −5.10V".
			Resolution near zero is much greater so that the level will change slower as zero is approached and passed.
	Control knob	Rotate CW until display indicates "OFFSET 0.0 mV".	
	F1 (AMPL)	Press once	
	Control knob	Rotate CW until display indicates "AMPL 5.000 Vp".	
	This step verifies the "Frequency" functions of the Model 75.		
8			Connect a coax cable from the Ref Out connector on the Model 75 rear panel to the frequency counter input. Set frequency counter to frequency mode.
	Parameter	Press two times	
	F3 (SAMPL)	Press once	Display will indicate "SAMPL 1.0000 MHz" and counter will indicate approximately 1 MHz.
	Control knob	Rotate CCW until display indicates "SAMPL 500.0 KHZ".	Counter will indicate approximately 500 kHz.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
8 (Cont)	Control knob	Rotate CCW until display indicates "SAMPL 300.0 KHZ".	Counter will indicate approximately 300 kHz.
	Control knob	Rotate CCW until display indicates "SAMPL 100.00 KHZ".	Counter will indicate approximately 100 kHz.
	Control knob	Rotate CCW until display indicates "SAMPL 10.000 KHZ".	Counter will indicate approximately 10 kHz.
	Control knob	Rotate CCW until display indicates "SAMPL 1.0000 KHZ".	Counter will indicate approximately 1kHz.
	Control knob	Rotate CCW until display indicates "SAMPL 100.00 HZ".	Counter will indicate approximately 100 Hz. Set frequency counter to measure period.
	Control knob	Rotate CCW until display indicates "SAMPL 10.000 HZ".	Counter will indicate approximately 100 ms.
	Control knob	Rotate CCW until display indicates "SAMPL 1.0000 HZ".	Counter will indicate approximately 1 sec.
	Control knob	Rotate CCW until display indicates "SAMPL 100.00 mHZ".	Counter will indicate approximately 10 sec.
	Control knob	Rotate CW until display indicates "SAMPL 1.0000 KHZ".	Oscilloscope will indicate a slow sine wave of 10 Vp-p.
This step verifies the "Hold" functions of the Model 75.			
9	Hold	Press once	Display indicates "HOLD:ON". Oscilloscope indicates that waveform stops at instantaneous dc level.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
9 (Cont)	Hold	Press once	Oscilloscope waveform starts again.
			Connect a coax cable from the TTL source output to the Hold In connector on the Model 75 rear panel.
		Apply a TTL low or switch closure input connector.	Oscilloscope indicates that waveform stops at instantaneous dc level.
		Remove the TTL low or switch closure from the rear panel connector.	Oscilloscope indicates that waveform starts again.
		This step verifies the "Return" functions of the Model 75.	
10	Return	Press once	Oscilloscope indicates that waveform stops at instantaneous dc level and moves slowly to approximately 0 Vdc. Display indicates "HOLD:ON Y = 0000".
	Hold	Press once	Oscilloscope waveform starts again. Display indicates "HOLD:OFF".
			Connect a coax cable from the TTL source output to the Return In connector on the Model 75 rear panel.
		Apply a TTL low or switch closure input to the rear panel connector.	Oscilloscope indicates that waveform stops at instantaneous dc level and moves slowly to approximately 0 Vdc. Display indicates "HOLD:ON Y = 0000".
			Remove the TTL low or switch closure input from the rear panel connector.
	Hold	Press once	Oscilloscope indicates that waveform starts again.
		This step verifies the "Mode" functions of the Model 75.	
11	Parameter	Press two times	
	F1 (MODE)	Press once	
	Control knob	Rotate CW until display indicates "MODE TRIGGERED".	Oscilloscope trace level approximately 0 Vdc. Set oscilloscope sweep to .5 sec/DIV.
	Trigger	Press once	Oscilloscope waveform runs for one cycle, then stops at 0 Vdc.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
11 (Cont)	Control knob	Rotate CW until display indicates "MODE GATED".	
	Trigger	Press and hold	Oscilloscope waveform runs continuously.
	Trigger	Release	Oscilloscope waveform stops at 0 Vdc.
	Control knob	Rotate CW until display indicates "MODE TOGGLED".	
	Trigger	Press once	Oscilloscope waveform runs continuously.
	Trigger	Press once	Oscilloscope waveform stops at 0 Vdc.
	F3 (BURST)	Press once	
	Control knob	Rotate CCW until display indicates "BURST CT 3".	
	F1 (MODE)	Press once	
	Control knob	Rotate CW until display indicates "MODE BURST".	
	Trigger	Press once	Oscilloscope waveform runs for 3 cycles, then stops at 0 Vdc.
	Counter	Press once	Display will indicate "COUNTER = 3".
This step verifies the "Burst Done Out" signal of the Model 75.			
12			Connect a cable from Burst Done Out connector to oscilloscope CH 2 vertical input. Reset oscilloscope vertical input to CHOPPED with CH1 and CH2 both "On" and at 2V/DIV.
	Trigger	Press Once	Oscilloscope Burst Done Out signal goes to 0 Vdc while waveform is running and then returns to +5V when waveform stops.
This step verifies the "Trig In" functions of the Model 75.			
13			Connect the Model 75 as shown in figure 2-12. Set equipment controls as indicated in table 2-9.

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
13 (Cont)	F1 (MODE)	Press once	
	Control knob	Rotate CW until display indicates "MODE TRIGGERED".	
	Parameter	Press once	
	F1 (FREQ)	Press once	
	Control knob	Rotate CW until display indicates "FREQ 900.00 HZ".	Oscilloscope displays one cycle of sine wave whose start is coincident with rising edge of the trigger signal.
This step verifies the "Trigger Slope" function of the Model 75.			
14	Parameter	Press two times	
	F2 (TRSLP)	Press once	
	Control knob	Rotate CW until display indicates "TRIG SLOPE NEG".	Oscilloscope displays one cycle of sine wave whose start is coincident with falling edge of the trigger signal.
This step verifies the "Sync In" functions of the Model 75.			
15	F1 (MODE)	Press once	
	Control knob	Rotate CCW until display indicates "MODE CONTINUOUS".	Move the cable from the Trig In connector to the Sync In connector. Oscilloscope waveform runs continuously when the Sync In signal is low. Waveform goes to 0 Vdc when Sync In is high.
This step verifies the "Ref In" functions of the Model 75.			
16			Connect the Model 75 as shown in figure 2-13. Set equipment controls as indicated in table 2-10.
	Parameter	Press two times	

Table 2-6. Checkout Procedure (Continued)

Step	Control/Switch	Position/Operation	Observation/Comments
16 (Cont)	F3 (REF)	Press once	
	Control knob	Rotate CW until display indicates "REF EXTERNAL".	
	TTL Signal source	Vary the frequency up and down.	Oscilloscope waveform frequency varies with the TTL frequency.
	This step verifies the "Sum In" functions of the Model 75.		
17			Connect the Model 75 as shown in figure 2-14. Set equipment controls as indicated in table 2-11.
	Control knob	Rotate CW until display indicates "REF INTERNAL".	
	Edit	Press two times	
	F1 (FUNC)	Press once	
	Control knob	Rotate CW until display indicates "FUNC DC".	
	F3 (EXEC)	Press once	Oscilloscope (CH1) waveform is the same frequency and approximately the same amplitude as the (CH2) waveform.

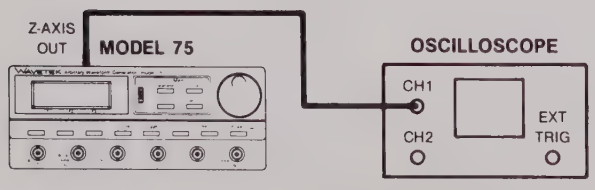


Figure 2-10. Equipment Interconnection #1

Table 2-7. Test Equipment Control Setup#1

Oscilloscope	
CH1 Vert Input	5 V/DIV
Horiz Sweep	.5 ms/DIV
Trigger Source	CH1
Trigger Mode	Auto
Remaining Controls	As Required

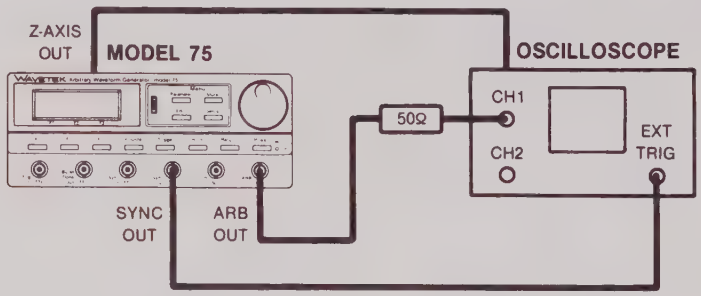


Figure 2-11. Equipment Interconnection #2

Table 2-8. Test Equipment Control Setup #2

Oscilloscope	
CH1 Vert Input	2 V/DIV
Horiz Sweep	.5 ms/DIV
Trigger Source	Ext (÷ 10 if available)
Trigger Mode	Auto
Trigger Slope	Positive
Trigger Coupling	AC
Remaining Controls	As Required

Table 2-9. Equipment Control Setup #3

TTL Signal Source		Oscilloscope	
Frequency	200 Hz	CH1 Vert Input	2 V/DIV
Function	TTL	CH2 Vert Input	2 V/DIV
		Vert Mode	Alt
		Horiz Sweep	.5 ms/DIV
		Trigger Source	CH2
		Trigger Mode	Auto
		Trigger Slope	Positive
		Trigger Coupling	AC
		Remaining Controls	As Required

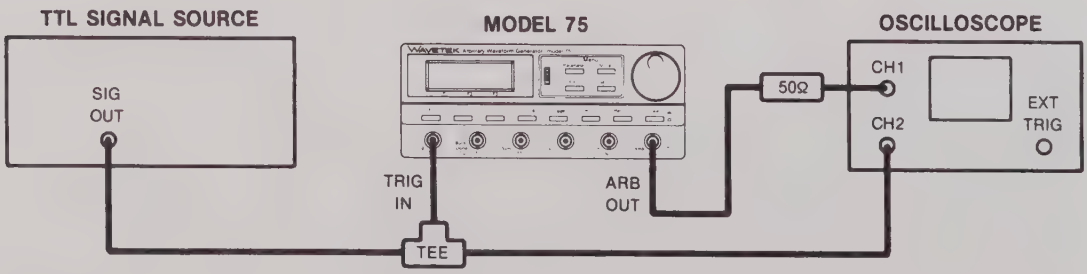


Figure 2-12. Equipment Interconnection #3

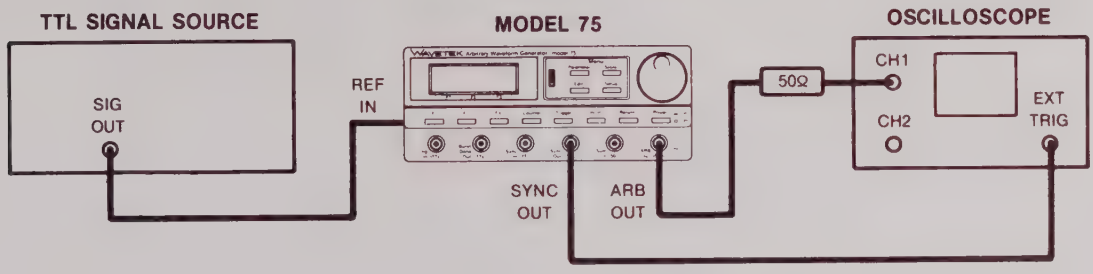


Figure 2-13. Equipment Interconnection #4

Table 2-10. Test Equipment Control Setup #4

TTL Signal Source		Oscilloscope	
Frequency	1 MHz	CH1 Vert Input	2 V/DIV
Function	TTL	Trigger Source	Ext (÷ 10 if avail)
		Horiz Sweep	.5 ms/DIV
		Trigger Mode	Auto
		Trigger Slope	Positive
		Trigger Coupling	AC
		Remaining Controls	As Required

Table 2-11. Test Equipment Control Setup #5

Signal Source		Oscilloscope	
Frequency	1.00 KHz	CH1 Vert Input	2 V/DIV
Function	Square Wave	CH2 Vert Input	2 V/DIV
Amplitude	10 Vp-p	Vert Mode	Alt
		Horiz Sweep	.2 ms/DIV
		Trigger Source	CH2
		Trigger Mode	Auto
		Trigger Slope	Positive
		Trigger Coupling	AC
		Remaining Controls	As Required

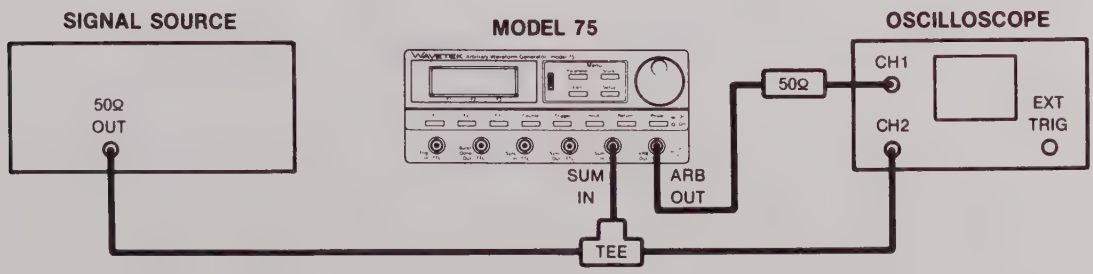


Figure 2-14. Equipment Interconnection #5

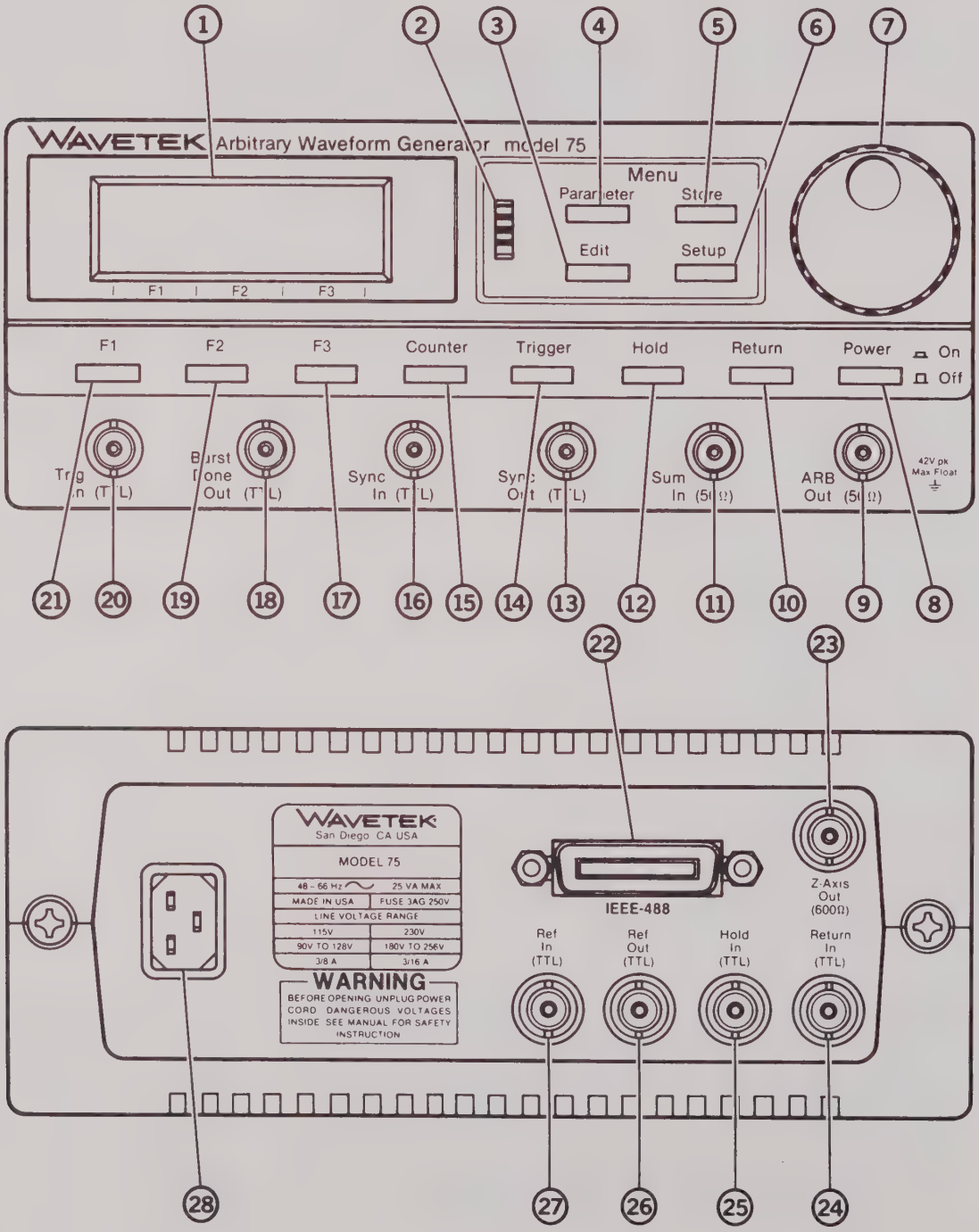


Figure 3-1. Controls, Connectors, and Indicators

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes the operation of the Model 75. Paragraph 3.2 describes the controls and connectors of the instrument. The following paragraphs describe how to use the various features and modes of the Model 75.

3.2 CONTROLS, CONNECTORS, AND INDICATORS

The front panel controls are organized into four menu selection keys, three soft keys, three real time keys, the Counter key, and the Control knob. To change any instrument setting, the appropriate menu key is pressed repeatedly until the desired soft key label appears in the bottom line of the display (see Appendix B for menu organization). Pressing the associated soft key will cause the top line of the display to indicate the setting to be changed. Rotating the Control knob will change the setting. When the setting being changed has the possibility of irreversibly changing a waveform, an execute label (EXEC) will appear for the F3 soft key and must be pressed before the change takes place. The Trigger, Hold, and Return keys control the waveform in real time and are not directly associated with the Control knob. The Counter key causes the display to indicate a waveform count as will be discussed below. The front panel controls and connectors are shown in figure 3-1 and keyed (bold numbers) to the following descriptions.

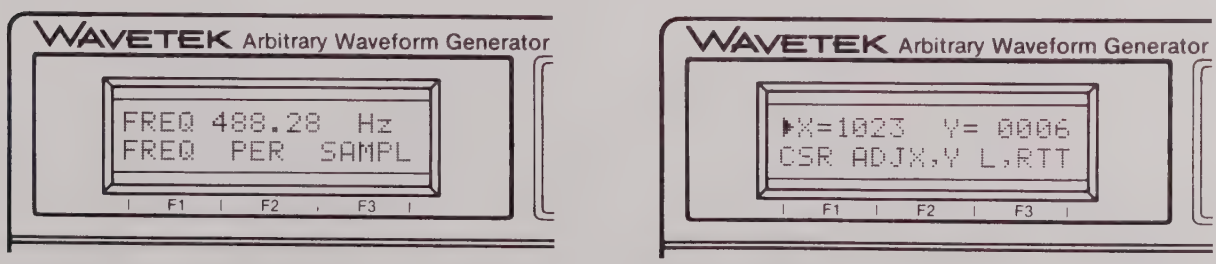
1 **Liquid Crystal Display** (See figure 3-2). The lower row of this display will provide labels for the soft keys that are located directly below the display. Each time one of the menu keys is pressed the labels will be updated to match the menu selection (see Appendix B). The upper row of the display will respond to the soft keys and control knob by indicating the setting or parameter value corresponding to the last soft key that was pressed.

2 **LCD Viewing Control.** This control allows the user to adjust the intensity of the display to match the viewing angle of the instrument.

3 **Edit Key.** Each time the edit key is pressed the lower line of the display will change to indicate three different waveform editing options. There are a total of five different sets of three editing options. Any of these can be invoked by pressing the soft key [F1 (21), F2 (19), or F3 (17)] below the corresponding label on the display.

NOTE

Refer to appendix B for a summary of soft key options.



FREQ SELECTED FROM PARAMETER MENU

ADJX SELECTED FROM EDIT MENU

Figure 3-2. Typical Display Indications

Pressing the Edit key the first time enables the rubber band editing features as follows:

The label for the F1 soft key will read "CSR" (Cursor). Pressing F1 allows the cursor in the waveform to be moved by rotating the control knob. The top line of the display will indicate the X-position of the cursor and the Y-value at that position. If Z-axis modulation is used on an oscilloscope, the cursor will be intensified. This does not affect the output waveform.

The label for the F2 soft key will read "ADJX,Y" (Adjust X or Y). Pressing F2 once allows a vertex (at the cursor position) of a waveform to be moved horizontally (X) by rotating the control knob. Pressing the F2 key twice allows vertical (Y) movement. The top line of the display will indicate the X and Y position of the vertex (cursor) and also (with an annunciator) the adjustment axis (X or Y) currently enabled

The label for the F3 soft key will read "L,RTT" (Left or Right Thumbtack). Pressing F3 once allows the horizontal position of the left thumbtack to be changed by rotating the control knob. Pressing the F3 key twice allows the horizontal position of the right thumbtack to be changed. The position of both thumbtacks will be indicated on the top line of the display along with an annunciator indicating the thumbtack whose adjustment is currently enabled. If Z-axis modulation is used on an oscilloscope, the thumbtacks will be intensified.

Pressing the Edit key the second time enables the standard waveform features as follows:

The label for the F1 soft key will read "FUNC" (Function). Pressing F1 allows standard waveforms to be inserted between the current thumbtacks (as set by L,RTT). The desired standard waveform is selected by rotating the control knob and is inserted when the EXEC soft key is pressed as discussed below.

The label for the F2 soft key will read "ERASE". Pressing this key followed by the EXEC soft key will erase the entire active waveform by changing all Y-values to 0.

The label for the F3 soft key will read "EXEC". (Execute). Pressing F3 causes the action selected by the FUNC or ERASE keys to be executed. An "X" will be be displayed in the top right hand corner of the display after EXEC has been pressed.

Pressing the Edit key a third time enables the digital amplitude and offset features as follows:

The label for the F1 soft key will read "DAMPL" (Digital Amplitude). Pressing F1 allows adjustment, by rotating the control knob, of the amplitude of the portion of the waveform between the thumbtacks without affecting the rest of the waveform. To accomplish this, the Model 75 digitally scales the Y-values of the waveform points between the thumbtacks. The top line of the display will indicate the amplitude of the portion being adjusted as a percentage of full scale. The digital amplitude can be adjusted to a negative relative amplitude in order to invert a portion of the waveform.

The label for the F2 soft key will read "DOFF" (Digital Offset). Pressing F2 allows a portion of the waveform between the thumbtacks to be offset vertically, by rotating the control knob, without affecting the rest of the waveform. The Model 75 accomplishes this by adding (or subtracting) a fixed value to all of the points between the thumbtacks. The range of digital offset adjustment is limited by the fact that the Y-value of any point cannot be outside the range of ± 2047, so the Model 75 will not allow this range to be exceeded. The top line of the display will indicate the offset, in points, relative to the original position, of the portion being adjusted.

The label for the F3 soft key will read "L,RTT" (Left or Right Thumbtack). Pressing F3 once allows the horizontal position of the left thumbtack to be changed by rotating the control knob. Pressing F3 twice allows the horizontal position of the right thumbtack to be changed. The position of both thumbtacks will be indicated on the top line of the display along with an annunciator indicating the thumbtack whose adjustment is currently enabled. Moving the thumbtacks has no effect on the output waveform. If Z-axis modulation is used on an oscilloscope, the thumbtacks will be intensified.

Pressing the Edit key a fourth time enables start/stop address control and the waveform normalization function as follows:

The label for the F1 soft key will read "START" (Start Address). Pressing F1 allows setting, by rotating the control knob, of the address of the first waveform memory location to be part of the active waveform. The top line of the display will indicate both the current start and stop addresses along with an annunciator indicating that START has been pressed.

The label for the F2 soft key will read "STOP" (Stop Address). Pressing F2 allows setting, by rotating the control knob, of the address of the last waveform memory location to be part of the

active waveform. The top line of the display will indicate both the current start and stop addresses along with an annunciator indicating that START has been pressed.

The label for the F3 soft key will read "NORML" (Normalize). Pressing the F3 key scales the portion of the waveform between the thumbtacks so that its peak Y-value is either ±2047. This is exactly the same as using DAMPL and turning the control knob until "100%" is displayed. Normalizing a waveform ensures that its peak value will be as set by the amplitude parameter.

Pressing the Edit key a fifth time enables the single point editing features as follows:

The label for the F1 soft key will read "CSR" (Cursor). Pressing F1 allows the cursor in the waveform to be moved by rotating the control knob. The top line of the display will indicate the X-position of the cursor and the Y-value at that position. If Z-axis modulation is used on an oscilloscope, the cursor will be intensified. This does not affect the output waveform.

The label for the F2 soft key will read "INCRX" (Increment X Position). Pressing F2 causes the position of the cursor to increase by one. The top line of the display will indicate the X-position of the cursor and the Y-value at that position. This does not affect the output waveform.

The label for the F3 soft key will read "ADJYPT" (Adjust the Y-Value of a Point). The level of individual points of the waveform can be adjusted by pressing F3 and rotating the control knob. The top line of the display will indicate both the X position and Y value of the point.

Pressing the Edit key additional times will continuous cycle through the above options.

4 **Parameter Key.** Each time the Parameter key is pressed the lower line of the display will change to indicate three different parameter setting options. There is a total of three different sets of three parameter setting options. Any of these can be invoked by pressing the soft key [F1 (21), F2 (19), or F3 (17)] below the corresponding label on the display.

NOTE

Refer to appendix B for a summary of the soft key options.

Pressing the Parameter key the first time enables the control of the output frequency in three different ways. Each of these is actually settng the sample frequency (see paragraph 3.14.1), but the display will be in three different forms as follows:

The label for the F1 soft key will read "FREQ" (Waveform Frequency). Pressing F1 allows the frequency to be set using the control knob.

The label for the F2 soft key will read "PER" (Waveform Period). Pressing F2 allows the period to be set using the control knob.

The label for the F3 soft key will read "SAMPL" (Sample Frequency). Pressing F3 allows the sample frequency to be set using the control knob.

Pressing the Parameter key a second time enables amplitude-offset control and also allows the selection of external frequency reference as follows:

The label for the F1 soft key will read "AMPL" (Amplitude). Pressing F1 allows setting of the peak amplitude by rotating the control knob. The top line of the display will indicate the amplitude in volts peak (into 50Ω). See paragraph 3.14.3 for an explanation of the interrelation between amplitude and offset.

The label for the F2 soft key will read "OFFSET". Pressing F2 allows setting of the output offset voltage by rotating the control knob. The top line of the display will indicate the offset in volts (into 50Ω). See paragraph 3.14.4 for an explanation of the interrelation between amplitude and offset.

The label for the F3 soft key will read "REF" (Frequency Reference). Pressing F3 allows selection of either the internal synthesizer (as set by FREQ, PER, or SAMPL) or an external signal (Ref in connector-27) by rotating the control knob.

Pressing the Parameter a third time enables the mode controls as follows:

The label for the F1 soft key will read "MODE". Pressing F1 allows selection of one of the five operating modes by rotating the control knob.

The label for the F2 soft key will read "TRSLP" (Trigger Slope). Pressing F2 allows the selection of the trigger slope polarity as either positive or negative by rotating the control knob.

The label for the F3 soft key will read "BURST" (Burst Count). Pressing F3 allows the setting of the number of waveform cycles to be output after each trigger in burst mode by rotating the control knob.

Pressing the Parameter key additional times will continuously cycle through the above options.

5 **Store Key.** Each time the Store key is pressed the lower line of the display will change to indicate one of two sets of three setting storage options. Setting

storage is only available for waveform lengths of 2048 points or less (see CHAIN below). Any of these can be invoked by pressing the soft key [F1 (21), F2 (19), or F3 (17)] below the corresponding label on the display.

NOTE

Refer to appendix B for a summary of the soft key options.

Pressing the Store key the first time enables the store and recall functions as follows:

The label for the F1 soft key will read "STORE". Pressing the F1 key, selecting one of the three locations with the control knob, then pressing EXEC key (see F3 below), will copy the current waveform and settings into the selected location. The previous contents of the selected location will be lost.

The label for the F2 soft key will read "RCALL" (Recall). Pressing the F2 key, selecting one of the three locations with the control knob, then pressing EXEC key (see F3 below), will copy the selected waveform and setting into the active instrument setup. The previous setup and waveform will be lost.

The label for the F3 soft key will read "EXEC" (Execute). Pressing F3 causes the action selected by the STORE or RCALL keys to be executed. An "X" will be displayed in the top right hand corner of the display after EXEC has been pressed.

Pressing the STORE key a second time will enable the exchange function and the chain option as follows:

The label for the F1 soft key will read "EXCHG" (Exchange). Pressing the F1 key, selecting one of the three locations with the control knob, then pressing EXEC key (see F3 below), will exchange the current waveform and settings with the selected location. In this way, neither waveforms nor settings are lost.

The label for the F2 soft key will read "CHAIN". The Chain function allows chaining the active waveform memory with the three waveform storage areas to produce waveforms longer than 2048 points. Pressing the F2 key, selecting "8K" with the control knob, then pressing EXEC key will chain the waveforms together. Pressing the F2 key, selecting "2K" with the control knob, then pressing "EXEC" key will unchain the waveforms and reenable waveform and setting storage.

The label for the F3 soft key will read "EXEC" (Execute). Pressing F3 causes the action selected by the EXCHG or CHAIN to be executed. An "X" will be displayed in the top right hand corner of the display after EXEC has been pressed.

Pressing the Store key additional times will continuously cycle through the above options.

6 **Setup Key.** Each time the Setup key is pressed the lower line of the display will change to indicate three different instrument setup options. There are a total of four different sets of three parameter setting options if no communications option (RS-232-C or IEEE-488) is installed or five sets if a communication option is installed. Any of these can be invoked by pressing the soft key [F1 (21), F2 (19), or F3 (17)] below the corresponding label on the display.

NOTE

Refer to appendix B for a summary of the soft key options.

Pressing the Setup key the first time enables the sync pulse and ramp rate controls as follows:

The label for the F1 soft key will read "SYNC". Pressing F1 allows the position of the pulse from the Sync Out connector (13) to by set to anywhere in the active waveform by rotating the control knob. The top line of the display will indicate this position by the waveform address and in degrees relative to the beginning of the waveform.

The label for the F2 soft key will read "PHASE". Pressing F2 allows the adjustment of the relative phase of different model 75s running in parallel by rotating the control knob. The top line of the display indicates the phase in degrees relative to the beginning of the waveform. This actually is moving the sync pulse just as in SYNC above, except that there is a two point offset in the degree reading on the display.

The label for the F3 soft key will read "RAMP" (Ramp to Start Rate). This is the rate at which the output ramps back to the start value when the "Return" feature is used. Pressing F3 allows this rate to be set by rotating the control knob.

Pressing the Setup key a second time enables the break point setting features as follows:

The label for the F1 soft key will read "CSR" (Cursor). Pressing F1 allows the cursor in the waveform to be moved by rotating the control knob. The top line of the display will indicate the X-position of the cursor and whether a break point is "on" or "off" at that position. If Z-axis modulation is used on an oscilloscope, the cursor will be intensified. This does not affect the output waveform.

The label for the F2 soft key will read "NEXTBP" (Go to Next Break Point). Pressing F2 will cause the cursor to jump to the next location where a break point is "on".

The label for the F3 soft key will read "TGLBP" (Toggle Break Point On/Off). Pressing F3 will turn a break point "on" if it is "off" or "off" if it is "on" at the current cursor position.

Pressing the Setup key a third time enables the break point clearing and reset functions as follows:

The label for the F1 soft key will read "CLRBPS" (Clear all Break Points). Pressing F1, then the EXEC key, will clear all of the currently set break points (turn them "off"), and insert the default break point at the start address.

The label for the F2 soft key will read "RSET" (Reset). Pressing F2, then the EXEC key, will reset the instrument to the defaults listed in table 3-1. This will not affect the active or stored waveforms. The top line of the display will indicate the software version number.

The label for the F3 soft key will read "EXEC" (Execute). Pressing F3 causes the action selected by the CLRBPS or RSET to be executed. An "X" will be displayed in the top right hand corner of the display after EXEC has been pressed.

Pressing the Setup key a fourth time enables the Z-axis and calibration controls as follows:

The label for the F1 soft key will read "ZLEVL" (Z-Axis Drive Level). Pressing F1 allows adjustment of the amplitude at the Z-axis output connector (23) by rotating the control knob. The top line of the display indicates this level in volts. Refer to paragraph 3.5 for a procedure for setting up Z-axis modulation.

The label for the F2 soft key will read "ZLOGIC" (Z-Axis Logic Polarity). Pressing F2 allows setting of the Z-axis output (23) to either positive (high = bright) or negative (low = bright) by rotating the control knob. Refer to paragraph 3.5 for a procedure for setting up Z-axis modulation.

The label for the F3 soft key will read "CAL" (Calibration). Pressing F3 allows the calibration of the output offset. Refer to section 5 for the calibration procedure.

Pressing the Setup key a fifth time enables the communication option controls if a communication option is installed. Refer to paragraph 3.26 (IEEE-488) or 3.30 (RS-232-C) for more information about these controls.

Pressing the Setup key additional times will continuously cycle through the above options.

7 **Control Knob.** Used to change the value or selection associated with the three soft key. The top line of the display will display the value or selection made by the control knob.

8 **Power Switch.** This switch turns the instrument On or Off. At power-on, the instrument initializes to the conditions existing when the instrument was last turned off.

9 **ARB Out (50Ω) Connector.** This BNC connector is the main output for the ARB waveform. The maximum voltage output amplitude is ± 5 Vp into a 50Ω load. This connector is internally fuse protected.

10 **Return Key.** Pressing the Return key causes the output to ramp back to the starting "Y" value. The rate of the ramp is adjustable from 0 to 100 ms per vertical point. If the instrument is in Continuous mode, the output will be held after the return and can be restarted by pressing the Hold key. If the waveform is in the Trigger, Gate, Toggle, or Burst mode, the output will wait for another trigger (manual or external) before restarting.

11 **Sum in (50Ω) Connector.** Provides a means of inputting an external waveform to be summed with the ARB internal waveform. This input is fuse protected against accidental application of high voltage. A ± 5Vp input will produce an output equal to the amplitude setting at the "ARB Out" connector. The sum of this signal and the internal waveform cannot exceed ± 5 Vp.

12 **Hold Key.** This key, when pressed, will stop the waveform at the ARB Out connector and hold the output at the instantaneous (when pressed) value of "Y". Pressing the Hold key a second time will continue the original waveform.

13 **Sync Out (TTL) Connector.** This connector provides a sync signal for synchronizing an oscilloscope or another ARB generator with this ARB generator. The waveform from this connector is a pulse one sample time wide. The position is adjustable to anywhere in the waveform.

14 **Trigger Key.** This key allows the waveform to be manually controlled in four different ways depending on the mode. The trigger slope polarity (TRSLP) is settable as either positive or negative.

1. When in the Triggered Mode the generator will output one cycle of the waveform each time the key is pressed.

2. When in the Gated Mode the generator will output a continuous waveform as long as the key is pressed. When the key is released the waveform will cease.
3. When in the Toggle Mode, pressing the key once will output a continuous waveform. Pressing the key a second time will stop the waveform output.
4. When in the Burst Mode, the generator will output the preset number of cycles.

15 **Counter Key.** When in the Gated, Toggled, or Burst Modes pressing this key will indicate the number of complete cycles of the waveform that have been output since the last trigger.

16 **Sync In (TTL) Connector.** Primarily used for synchronizing several arbitrary waveform generators in parallel. A high level at this input causes the waveform to restart operation at the start address.

17 **F3 Key.** This is a soft key that allows selection of the option displayed directly above it. The function of this key is changed by the menu keys (3, 4, 5, and 6). The top line of the display will respond to the key being pressed.

For some menus, the F3 soft key (17) will have an "EXEC" label. Pressing the F3 soft key will cause the condition or value set by the F1 or F2 soft key to be entered (executed).

18 **Burst Done Out (TTL) Connector.** This output is low during active waveform output and high while waiting for a trigger in Trig, Gate, Toggle, and Burst modes. It is primarily used as the trigger source to start another ARB generator in series operation.

19 **F2 Key.** This is a soft key that allows selection of the option displayed directly above it. The function of this key is changed by the menu keys (3, 4, 5, and 6). The top line of the display will respond to this key being pressed.

20 **Trig In (TTL) Connector.** This connector provides for an external TTL signal input to control the generator in the Trigger, Gate, Toggle, and Burst modes. The slope polarity (TRSLP) is settable.

21 **F1 Key.** This is a soft key that allows selection of the option displayed directly above it. The function of this key is changed by the menu keys (3, 4, 5, and 6). The top line of the display will respond to this key being pressed.

22 **Communication Option Connector.** Either an IEEE-488 connector, an RS-232-C connector, or a blank cover plate will be mounted here depending on the option installed.

23 **Z-Axis Out (600Ω) Connector.** Used to modulate the Z-axis of an oscilloscope when using the waveform editing features. The level of this signal is menu selectable from 2 to 14 volts. Additional lower levels can be obtained by terminating the output into 50Ω. Logic polarity is also selectable.

24 **Return In (TTL) Connector.** A TTL low or switch closure applied at this input will cause the output to ramp back to the starting "Y" value. The rate of the ramp is adjustable from 0 to 100 ms per point. If the instrument is in Continuous mode, the output will be held after the return and can be restarted by pressing the hold key. If the waveform is in Trig, Gate, Toggle, or Burst, the output will wait for another trigger (manual or external) before restarting.

25 **Hold In (TTL) Connector.** A TTL low or switch closure signal at this input will cause the waveform to stop at the instantaneous "Y" value. A TTL high or open will cause the waveform to continue.

26 **Ref Out (TTL) Connector.** This connector outputs a TTL level pulse train at the sample frequency to synchronize other ARB generators in series or parallel operation.

27 **Ref In (TTL) Connector.** This connector allows the input of an external TTL level sample clock when external reference is selected.

28 **External Power Connector.** This connector allows the use of a standard 3-wire, UL listed/CSA certified, removable power cord.

NOTE

All outputs that are specified as "TTL" are defined as follows:

HIGH $V_{out} \geq 4.4V$ @ $I_{out} \leq 20\ \mu a$
$V_{out} \geq 3.8V$ @ $I_{out} \leq 4$ ma

LOW $V_{out} \leq 0.1V$ @ $I_{out} \leq 20\ \mu a$
$V_{out} \leq 0.33V$ @ $I_{out} \leq 4$ ma

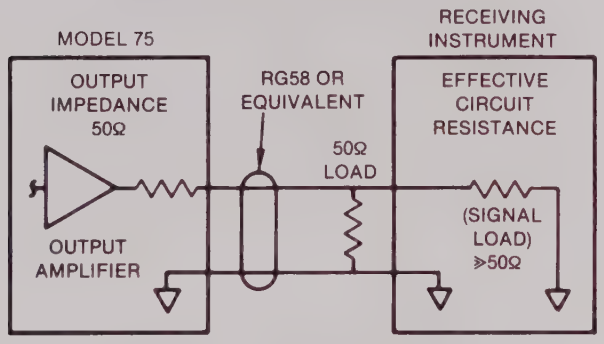


Figure 3-3. Signal Termination

3.3 OPERATION

The following paragraphs describe the various operational configurations and features of the Model 75. Descriptions of the individual controls and connectors may be found in paragraph 3.2.

Proper signal termination, or loading, of the ARB Out connector is necessary for its specified operation. Figure 3-3 shows the proper termination of the ARB Out connector with standard 50Ω output impedance. Placing the 50 Ω terminator, or 50Ω resistance, in parallel with a higher load impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

The impedances of the generator input and output connectors are:

Connectors	Impedance
ARB Out (50Ω)	50Ω
Sync Out (TTL)	N/A
Burst Done Out (TTL)	N/A
Ref Out (TTL)	N/A
Z-Axis Out (600Ω)	600Ω
Sum In (50Ω)	50Ω
Trig In (TTL)	100kΩ
Sync In (TTL)	100kΩ
Ref In (TTL)	100kΩ
Hold In (TTL)	100kΩ
Return In (TTL)	100kΩ

3.4 INITIAL SETUP

When power is turned on, Model 75 will assume the instrument setup conditions that were present when power was last turned off. If, when power is first turned on, the bottom line of the display reads "**COLD START**", memory has been lost due to a low battery and the instrument will need to be calibrated and set up again.

Before setting up the instrument, the instrument can be cleared (reset) to the default settings listed in table 3-1 by using the RSET soft key from the Setup menu. RSET will not affect calibration, Z-axis output, or any waveforms. To clear the old waveform, in order create a new one, the ERASE soft key from the Edit menu can be used. Resetting, then erasing, is normally the best way to start a new test setup. To use the RSET soft key, press the Setup key repeatedly until the RSET label is seen on the bottom line of the display and then press the RSET soft key (F2) followed by the EXEC soft key (F3).

Table 3-1. Model 75 Default Conditions

Sample Frequency: 1.0000 MHz
Frequency: 488.28 Hz
Period: 2.0480 ms
Amplitude: 5.000 Vp
Offset: 0.00V
Reference: Internal
Mode: Continuous
Trigger Slope: Positive
Burst: 8
Cursor: X = 1023
Left Thumbtack: 0000
Right Thumbtack: 2047
Function: DC
Start Address: 0000
Stop Address: 2047
Sync Address: 0000 0.00°
Phase Difference: 0.35°
Ramp Time: 5 ms/bit
Z Level: (Not Affected)
Z Logic: (Not Affected)
Chain: 2K
Hold: Off

3.5 EDITING WAVEFORMS

Waveform editing is best accomplished using an oscilloscope with Z-axis modulation to emphasize the "thumbtacks" and "cursor" used by the editing features. Oscilloscope Z-axis inputs vary widely in maximum input voltage and polarity. Consult your oscilloscope manual for the limits and then use the following procedure.

1. Setting the Z-axis logic polarity.
   a. If a high level reduces the intensity of your oscilloscope, then set the "ZLOGIC" polarity to "NEG" using the ZLOGIC soft key (from the Setup menu) and the Control knob.
   b. If a high level increases the intensity of your oscilloscope, then set the "ZLOGIC" polarity to "POS" using the ZLOGIC soft key (from the Setup menu) and the Control knob.

2. Setting the Z-axis voltage level.

   The Z-axis output has a fixed low level of approximately 0.2 volts and a high level that is adjustable to approximately 2, 4, 6, 8, 10, 12, or 14 volts. If your oscilloscope can be damaged by any of these Z-axis output levels, be sure that you do not exceed the maximum for your oscilloscope. This output can be loaded with a 50Ω feedthrough termination to reduce these levels by approximately a factor of 10.

   Set the timebase on the oscilloscope to show one or more waveform periods, then use the following procedure to adjust the Z-axis output and oscilloscope intensity for best viewing.

   a. With no feedthrough termination, set the Z-axis level to 2 volts using the ZLEVL soft key (from the Setup menu). Connect the Z-axis output cable to the oscilloscope.
   b. Adjust the oscilloscope intensity to the desired brightness.
   c. If the contrast between the bright dots (thumbtacks and cursor) and the rest of the waveform is too high, add a 50Ω feedthrough termination and return to step b. Alternately adjust the ZLEVL and oscilloscope intensity until the brightness and contrast are as desired.

3.6 THUMBTACKS AND CURSOR

Most of the waveform editing features use "thumbtacks" for defining the portion of the waveform to be edited. The thumbtacks are marked by pulses on the Z-axis output and therefore show up as bright dots on an oscilloscope waveform if Z-axis modulation is used. The position of the thumbtacks is adjusted by using the L,RTT soft key from the Edit menu. Pressing this soft key the first time enables adjustment of the left thumbtack (lower address) with the Control knob. Pressing the soft key additional times alternates between enabling adjustment of the right thumbtack and the left thumbtack. A cursor is used for "point" and "rubber band" editing. The position of the cursor can be adjusted by selecting the CSR soft key (from the Edit menu). The cursor is also marked by a pulse on the Z-axis output and will show up as a bright dot on the oscilloscope display.

3.7 RUBBER BAND EDITING

"Rubber band" editing is analogous to stretching a rubber band from one thumbtack, to the cursor, and then to a second thumbtack. To use this editing method, place the left and right thumbtacks on each side of the portion of the waveform to be edited (use L,RTT), then use the ADJX,Y soft key and Control knob to move the vertex either in the X (horizontal) or Y (vertical) direction. The CSR soft key can be used to pre-position the cursor (without changing the waveform) before using the ADJX,Y function. This is useful for editing the waveform while the Model 75 is connected to a system under test.

3.8 INSERTING STANDARD WAVEFORMS

Standard waveforms (sine, cosine, haversine, inverse sine, triangle, square, ramp up, ramp down, dc) are inserted between the thumbtacks using the FUNC soft key (from the Edit menu). When a standard waveform is inserted, it will be at full amplitude (as set by AMPL parameter) and centered around the offset voltage (as set by the OFFSET parameter). The relative amplitude and offset can be adjusted using "DAMPL" and "DOFF" as described in paragraphs 3.9 and 3.11. To insert a standard waveform:

1. Set the desired end points using the L,RTT soft key (from the Edit menu).
2. Press the FUNC soft key (from the Edit menu) and use the Control knob to select the desired waveform.
3. Press the EXEC soft key to insert the waveform.
4. Use "DAMPL" and "DOFF" as described in paragraphs 3.9 and 3.11 to change the relative amplitude and offset of the inserted waveform if necessary.

3.9 DIGITAL AMPLITUDE

The "Digital Amplitude" editing feature allows adjustment of the amplitude of a portion of the waveform relative to the rest of the waveform. The waveform consists of a 4095 point high window with an amplitude controlled by the "AMPL" parameter. The "DAMPL" editing feature adjusts the amplitude of a portion of the waveform relative to this window. The change in amplitude is referenced to the left thumbtack as the zero point. The digital amplitude feature is not available in chained operation (waveforms longer than 2048 horizontal points). To use digital amplitude, set the end points of the section to be edited using the L,RTT soft key (from the Edit menu), press the DAMPL soft key, and then use the Control knob to adjust the amplitude. The digital amplitude can be adjusted past zero to negative amplitude to invert a portion of the waveform.

3.10 NORMALIZING

Pressing the "NORML" soft key from the "EDIT" menu, scales the portion of the waveform between the thumbtacks such that the peak value will be + 2047 or − 2047 points. This is equivalent to adjusting the digital amplitude to full scale.

3.11 DIGITAL OFFSET

"Digital Offset" is similar to digital amplitude, but is used to adjust the offset of a portion of the waveform relative to the rest of the waveform. To use digital offset, set the left and right thumbtacks (L,RTT soft key from the Edit menu) to the ends of the portion to be offset, press the DOFF soft key, and then use the Control knob to adjust the offset. When adjusting the digital offset, the Z-axis output is turned off to enable more accurate adjustment when viewing on an oscilloscope.

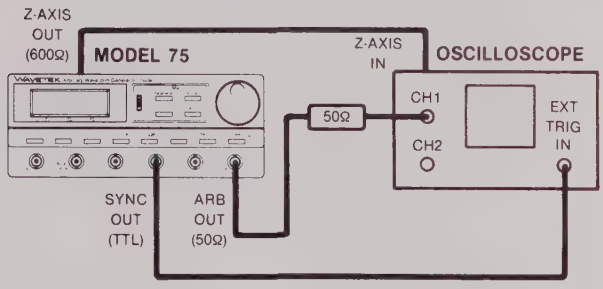
3.12 POINT EDITING

"Point" editing is used to edit individual points in a waveform. To edit individual points, press the Edit menu key repeatedly until "CSR INCRX ADJYPT" appears on the bottom line of the display. Press the CSR soft key (F1) and use the Control knob to move the cursor to the first point to be edited. Press the ADJYPT soft key (F3) and use the Control knob to adjust the "Y" value of the point. Pressing the INCRX soft key (F3) will increment the "X" value by 1, pressing ADJYPT a second time will re-enable adjustment of this next point. In this way successive points of the waveform can be edited by repeatedly pressing the INCRX, then ADJYPT soft keys and rotating the Control knob.

Example Setup

The following procedure produces a simulated medical "EKG" waveform.

1. Connect the equipment (Model 75 and the oscilloscope) as shown in the diagram.



   a. "ARB Out (50Ω)" through a 50Ω feedthrough termination to the vertical input of an oscilloscope.

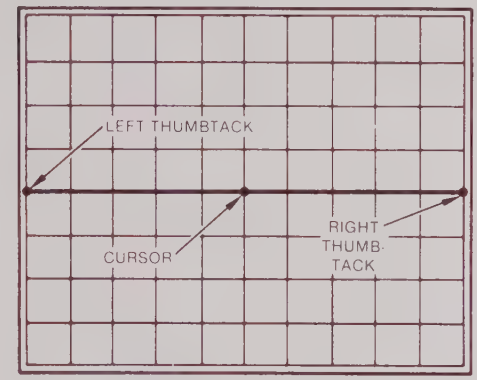
   b. "Sync Out (TTL)" to the external trigger input of the oscilloscope.

   c. "Z-Axis Out (600Ω)" to the Z-axis input of the oscilloscope. Use procedure in paragraph 3.5 to set the Z-axis intensity.

2. Set the Model 75 and oscilloscope controls as follows:

Model 75	**Oscilloscope**
Setup: Press 3 times	VERT INPUT: 2 V/DIV
F2 (RSET): Press once	VERT COUPLING: DC
F3 (EXEC): Press once	
Edit: Press two times	HORIZ SWEEP:
F2 (ERASE): Press once	.2 ms/DIV.
F3 (EXEC): Press once	TRIG MODE: AUTO
	TRIG COUPLING: AC
	TRIG SOURCE: EXT/10
	TRIG SLOPE/LEVEL: As Required
	INTENSITY: As Required by paragraph 3.5

3. The oscilloscope will now display a dc waveform of 0V with a left and right thumbtack and a cursor in the center as shown below.



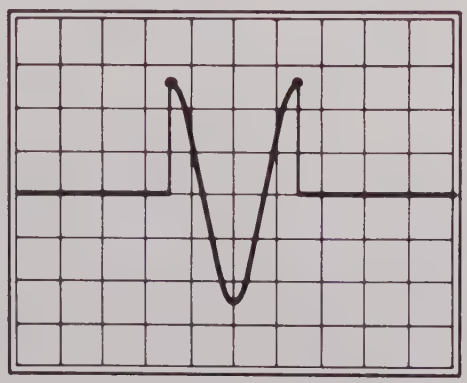
4. Some oscilloscope controls (depending on the make and model of oscilloscope used) may need to be adjusted slightly from the positions given in step 2.

   a. Adjust the oscilloscope horizontal trace (position control) to place the left thumbtack (intensity marker) at the left-hand edge vertical mark.

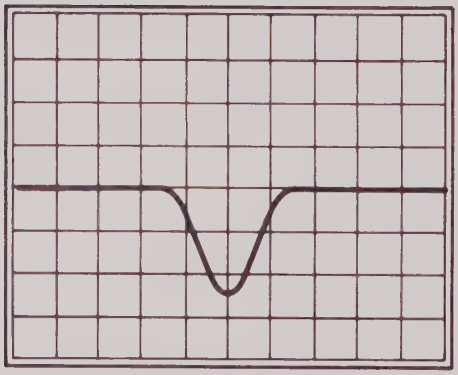
   b. Adjust the oscilloscope horizontal "VAR" control to place the right thumbtack at the right-hand edge vertical mark. One complete waveform cycle will then equal 10 divisions on the oscilloscope screen.

5.

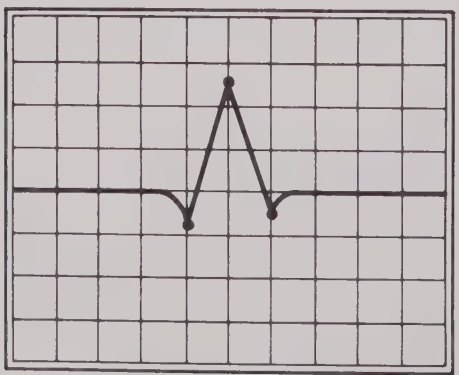
Edit:	Press four times
F3 (L,RTT):	Press once
Control Knob:	Rotate CW until the display indicates "> L = 0720"
F3 (L,RTT):	Press once
Control Knob:	Rotate CCW until the display indicates "> R = 1325"
Edit:	Press once
F1 (FUNC):	Press once
Control Knob:	Rotate CW until the display indicates "FUNC COSINE"
F3 (EXEC):	Press once



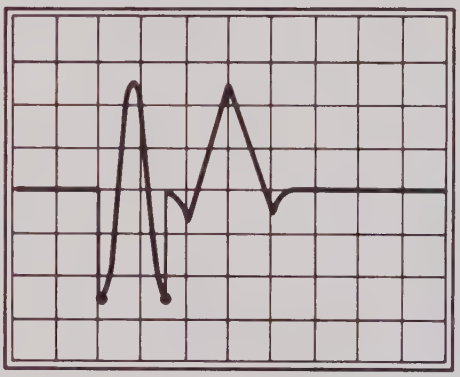
6. Edit: Press once.
F1 (DAMPL): Press once.
Control Knob: Rotate CCW until the display indicates "DIG AMPL 50%"
F2 (DOFF): Press once
Control Knob: Rotate CCW until the display indicates "DIG OFFSET −2047"



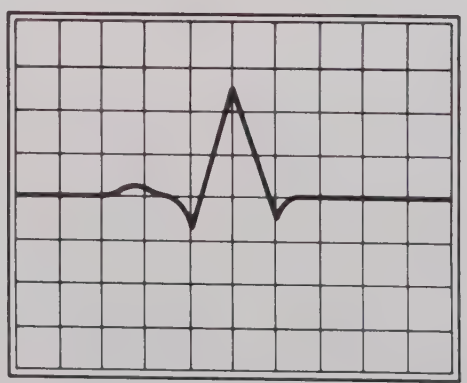
7. F3 (L,RTT): Press once
Control Knob: Rotate CW until the display indicates "> L = 0835"
F3 (L,RTT): Press once
Control Knob: Rotate CCW until the display indicates "> R = 1235"
Edit: Press three (3) times
F2 (ADJX,Y): Press two (2) times
Control Knob: Rotate CW until the display indicates "> Y = 2047"



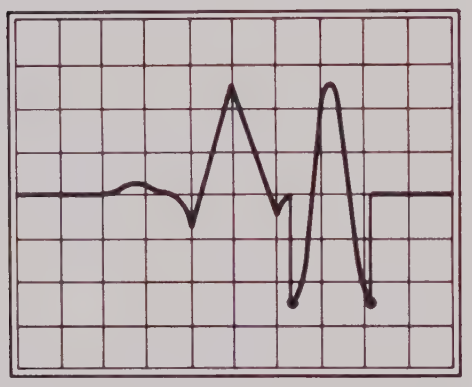
8. F3 (L,RTT): Press once
Control Knob: Rotate CCW until the display indicates "> L = 0410"
F3 (L,RTT): Press once
Control Knob: Rotate CCW until the display indicates "> R = 0730"
Edit: Press once
F1 (FUNC): Press once
Control Knob: Rotate CW until the display indicates "FUNC HAVER SINE"
F3 (EXEC): Press once



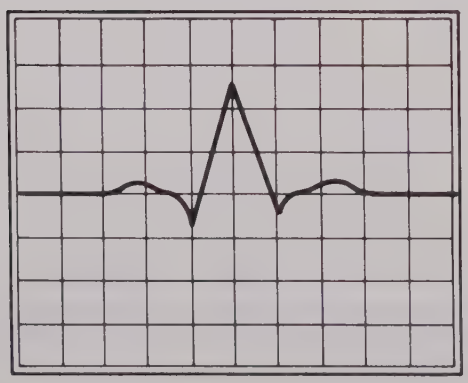
9. Edit: Press once
F1 (DAMPL): Press once
Control Knob: Rotate CCW until the display indicates "DIG AMPL 5%"
F2 (DOFF): Press once
Control Knob: Rotate CW until the display indicates "DIG OFFSET 2048"



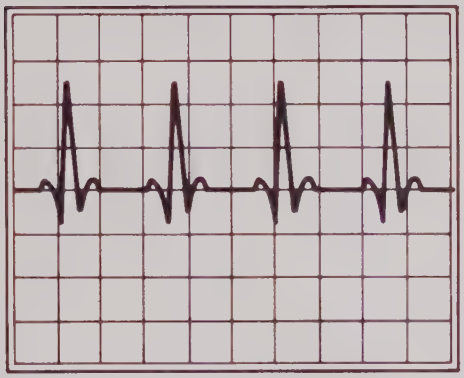
10. F3 (L,RTT): Press two (2) times
    Control Knob: Rotate CW until the display indicates "> R = 1680"
    F3 (L,RTT): Press once
    Control Knob: Rotate CW until the display indicates "> L = 1310"
    Edit: Press four (4) times
    F1 (FUNC): Press once
    F3 (EXEC): Press once



11. Edit: Press once
    F1 (DAMPL): Press once
    Control Knob: Rotate CCW until the display indicates "DIG AMPL 6%"
    F2 (DOFF): Press once
    Control Knob: Rotate CW until the display indicates "DIG OFFSET 2048"



12. Set the oscilloscope horizontal sweep to .5 ms/DIV. Adjust the horizontal sweep "VAR" control until the oscilloscope displays four (4) complete cycles of the waveform.



3.13 START AND STOP ADDRESSES

The "X" values at the beginning and end of the output waveform can be set to any value between 0 and 2047 points (8191 in chained operation) as long as the end is greater than the beginning. To set the beginning or end, press START or STOP (from the Edit menu) as desired and then use the Control knob to set the value. Break points after the stop address may be lost when moving the stop address.

3.14 WAVEFORM PARAMETERS

The "Parameter" menu allows changing of the frequency, amplitude, offset, and operational modes. The following four paragraphs will discuss the frequency, amplitude, and offset parameters. The operational modes will be discussed in paragraphs 3.15 thru 3.15.5.

3.14.1 Waveform Frequency, Period, and Sample Frequency

The waveform "frequency" can be set from the Parameter menu in one of three ways; in terms of "frequency" using the FREQ soft key (F1), in terms of "time period" using the PER soft key (F2), or in terms of "sample frequency" using the SAMPL soft key (F3). Adjusting any of these parameters is actually adjusting the "sample frequency", but the display is calibrated differently for each soft key. The waveform "frequency" is "sample frequency" divided by the number of horizontal "points" in the waveform. The waveform "period" is the inverse of the waveform "frequency". The number of points in the waveform is the stop address minus the start address plus one. To adjust any of these values, press the associated soft key and then use the Control knob to set the value.

3.14.2 External Reference

An external "clock" signal can be used as the main "sample frequency" by pressing the REF soft key (from the Parameter menu) and using the Control knob to select "REF EXTERNAL". The external clock signal is connected to the "Ref In" connector on the rear panel.

3.14.3 Waveform Amplitude

The waveform "amplitude" is displayed in volts peak. This amplitude is measured from the center of the waveform window (Y = 0) to the top or bottom of the waveform window (Y = ±2047). To set the amplitude, press the AMPL soft key (from the Parameter menu) and turn the Control knob as required. If the waveform does not reach the top or the bottom of the window the indicated amplitude will not be the actual amplitude of the output. The Normalize editing feature can be used to scale the waveform to match the amplitude setting. Move the thumbtacks to each end of the waveform and press the "NORML" soft key (from the Edit menu). The sum of the amplitude and offset settings automatically determines the best output attenuator range and therefore the offset setting will affect the resolution of the amplitude setting. The sum of the amplitude setting and the absolute value of the offset setting cannot exceed 5.2V.

3.14.4 Waveform Offset

The waveform "offset" is the voltage from zero to the center of the waveform window (Y = 0). To set the waveform offset, press the OFFSET soft key (from the Parameter menu) and use the Control knob to set the desired value. The sum of the amplitude and offset settings automatically determines the best output attenuator range and therefore the amplitude setting will affect the resolution of the offset setting. The sum of the amplitude setting and the absolute value of the offset setting cannot exceed 5.2V.

3.15 OPERATIONAL MODES

The Model 75 can operate in any one of five different modes. These are Continuous, Triggered, Gated, Toggled, or Burst. A description of each of these modes is given in paragraphs 3.15.1 thru 3.15.5. To change the operational mode, press the MODE soft key (from the Parameter menu) and use the Control knob to select the desired mode.

All of the modes except Continuous use a trigger to start the waveform output. The trigger can come from the Trigger key on the front panel, from the "Trig In" BNC connector on the front panel,or via the optional GPIB or RS-232-C interface. The polarity (slope) that causes the waveform to run can be set to either positive of negative by pressing the TRSLP soft key (from the Parameter menu) and turning the Control knob. When the trigger slope is set to positive, pressing the Trigger key or inputting a rising edge on the "Trig In" BNC will start the waveform. When the trigger slope is set to negative, releasing the Trigger key or inputting a falling edge on the "Trig In" BNC will start the waveform. If the "Trig In" BNC is held high, the polarity of the Trigger key will be reversed.

In all modes except Continuous, the waveform will stop and wait for another trigger only at the break points. By default, one break point is set at the beginning of the waveform. Break points can be set anywhere in the waveform or the default break point can be removed if desired. Setting and clearing break points will be discussed later.

NOTE

If all of the break points are removed from the waveform, then all of the modes will act like the Continuous mode.

3.15.1 Continuous Mode

In Continuous mode, the output runs repeatedly from the start address to the stop address. Neither the Trigger key or the "Trig In" BNC will have any effect in this mode.

3.15.2 Triggered Mode

In the Triggered mode, the waveform stops at a breakpoint and waits for a trigger from either the Trigger key or the "Trig In" input. When a trigger is received, the waveform runs until another break point is encountered, then stops and waits for another trigger. With only the default break point in the waveform, each trigger produces one waveform cycle.

3.15.3 Gated Mode

In the Gated mode, the waveform stops at a break point and waits for a trigger signal. When a trigger is received, the waveform runs until the trigger signal is removed and then stops at the next break point. If the trigger slope is set to negative, the waveform will start when the Trigger key is released or the "Trig In" input sees a high to low transition and runs until the Trigger key is pressed or the "Trig In" input goes high.

3.15.4 Toggled Mode

In the Toggled mode, the waveform stops at a break point and waits for a trigger signal. When a trigger is received, the waveform runs until a second trigger is received, then stops at the next break point. In this way, each trigger toggles the waveform "on" or "off".

3.15.5 Burst Mode

In the Burst mode, a trigger signal causes the generator to output a pre-determined number of waveforms (as set by the burst count) and stop at the next break point. To set the burst count, press the BURST soft key (from the Parameter menu) and use the Control knob to set a count from 1 to 1,048,575. Inputting another trigger signal during the burst sequence will cause the burst counter to start over.

3.16 SETTING AND CLEARING BREAK POINTS

To insert a "break point" into the waveform, press the CSR soft key (from the Setup menu) and then use the Control knob to position the cursor to the desired location in the waveform. The cursor position will be indicated numerically on the display and as a bright dot on a oscilloscope if the Z-axis modulation is used. Next, press the TGLBP soft key (from the Setup menu) to toggle the break point on. To remove a break point, move the cursor to the location of the break point either with the CSR soft key and the Control knob or by using the NEXTBP soft key. The NEXTBP soft key moves the cursor to the next break point. If there is a break point at the present cursor position, the display will indicate it with the word "ON" after the cursor address. All of the break points can be cleared and the default break point (X = 0000) inserted by pressing the CLRBPS soft key (from the Setup menu) followed by the EXEC soft key. For the operational modes to work correctly there must be at least one break point somewhere in the waveform. TGLBP both sets and clears breakpoints.

3.17 SYNC ADDRESS AND PHASE

Pressing the SYNC soft key (from the Set Up menu) allows the position of the pulse at the "Sync Out" output to be moved, anywhere relative to the waveform, by turning the Control knob. The display indicates the address and phase of the pulse. The PHASE soft key also allows the adjustment of the sync pulse, but the display indicates a phase that is offset by two sample times. This is used to adjust the relative phase of multiple instruments as discussed below under parallel operation.

3.18 STORING AND RECALLING WAVEFORMS

The Model 75 can hold three waveforms in storage in addition to the active waveform. Each of these waveforms can be up to 2048 samples long. To store a waveform, press the STORE soft key (from the Store menu), use the Control knob to choose the storage location, and then press the EXEC soft key to store. Recalling a waveform is done in the same way by using the RCALL soft key (from the Store menu). Storing or recalling a waveform erases either the stored waveform or the active waveform respectively. The EXCHG soft key (from the Store menu) can be used to exchange two waveforms without losing either one. Use the EXCHG soft key in the same manner as the STORE and RCALL soft keys.

3.19 CHAINED OPERATION

The "active" waveform can be chained with the three stored waveforms to create waveforms of up to 8192 samples long. When set for chained operation the entire waveform memory is active and no waveform storage locations are available. Also, the digital amplitude editing feature is not available. To set the instrument for chained operation, press the CHAIN soft key (from the Store menu), rotate the Control knob until "CHAIN 8K" is shown on the top line of the display, and then press the EXEC soft key. To set the instrument back to normal operation, perform the previous operation except rotate the Control knob to "CHAIN 2K". Chained operation can also be used to view the "active" waveform and the three stored waveforms in succession on an oscilloscope.

3.20 WAVEFORM COUNTER

Pressing the Counter key will cause the display to indicate a count of the number of waveforms that have been completed since the last trigger (up to a maximum of 1,048,575 waveforms). In Continuous and Triggered modes the counter is disabled. The counter can be read while the waveform is running or while the waveform is stopped such as after a gated or toggled sequence. In this way the length (in waveforms) of the last toggled or gated sequence can be displayed.

3.21 WAVEFORM HOLD

The output waveform can be held at its current level by using either the rear panel "Hold In" BNC or the front panel Hold key. Each time the Hold key is pressed the hold function is toggled on or off as indicated on the display. A TTL low level or a contact closure on the "Hold In" BNC holds the waveform and a high or open lets it run if the front panel Hold key is off.

3.22 RETURN TO START

Pressing the Return key on the front panel or a high to low transition (or switch closure) on the rear panel "Return In" BNC will cause the output to ramp from the current output level to the level at the start address. The rate of this ramp is adjustable from 0 to 100 ms per vertical step. 0 is a special case and causes the output to jump back to the start address level. To set the ramp rate, press the RAMP soft key (from the Setup menu) and use the knob to adjust it. In Continuous mode the hold will automatically be turned on at the end of the ramp and will need to be turned off with the Hold key to restart

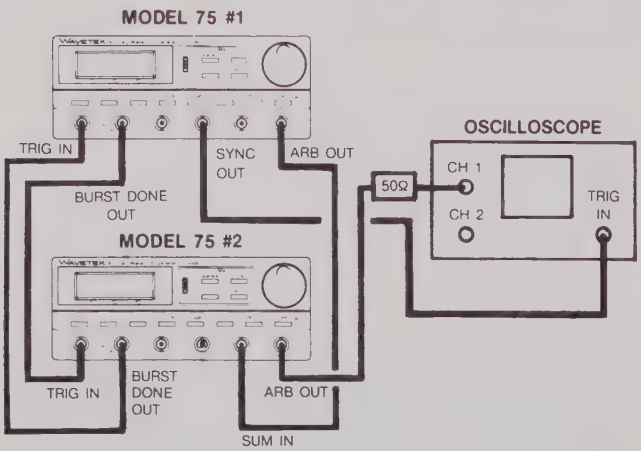
the waveform output. In all other modes the generator will be waiting for a trigger after the ramp to restart the waveform output.

3.23 LOW BATTERY INDICATOR

If the internal lithium battery runs low, the top line of the display will display "BAT" in addition to the normal message when a menu key is pressed. The low battery will not effect normal operation as long as the power is not turned off. If the power is turned off the instrument could lose all of the stored waveforms, setup information and calibration constant. If, when the power is first turned on, the bottom line of the display reads "**COLD START**", all of the memory has been lost due to a low battery and the instrument will need to be calibrated and set up again.

3.24 SERIES OPERATION

Several Model 75's can be connected in series (as shown in the following diagram), each one generating one or a burst of waveforms (see figure 3-4) and then triggering the next Model 75 in the chain. The outputs can be added together using the "Sum In" inputs to produce one waveform that is a chain of each of the individual waveforms in succession. This configuration can be used to create waveforms longer than the 8192 sample maximum or to create a series of normal waveforms followed by one or more abnormal waveforms.



To connect several Model 75's in series, the "Burst Done Out" connector of each Model 75 is connected to its successor's "Trig In". If the waveform is to run continuously, the last Model 75's "Burst Done Out" connector is connected back to the "Trig In" connector of the first. The "ARB Out" connector of each instrument is connected to its successor's "Sum In" connector and the last "ARB Out" connector is used as the main output. Each of the Model 75's can have independent waveform sample frequencies if desired, but if this is not necessary, one should be used as the master frequency reference. To do this, connect the "Ref Out" connector of the master frequency reference to the "Ref In" connector of all of the other Model 75's and set them for external reference. By doing this, the one sample time jitter between successive waveforms is eliminated.

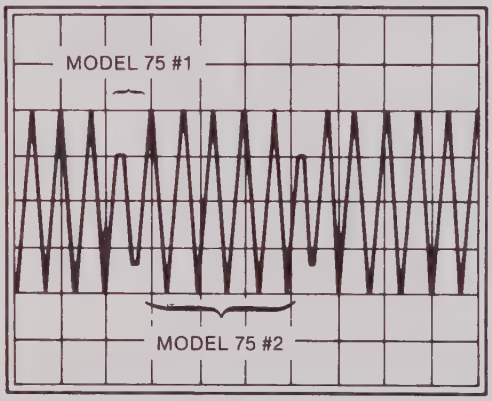


Figure 3-4. Example of Series Waveform

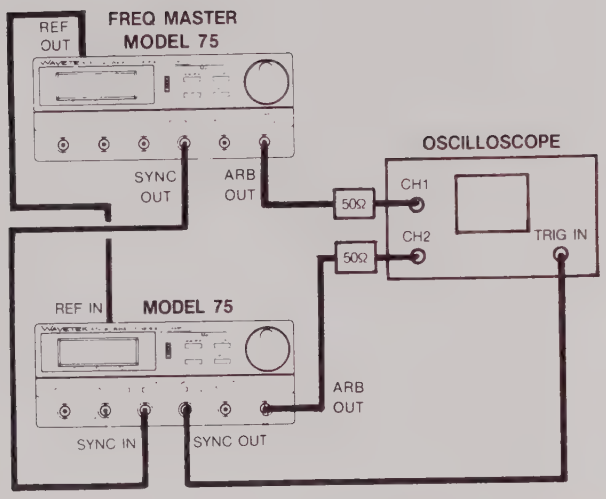
Each Model 75 should be set to either triggered (if it will be outputting one period of its waveform) or burst mode if it will be outputting a sequence of waveforms. The amplitude control of each Model 75 controls not only its own amplitude but the amplitude of the output due to the "Sum In" signal. A ±5V signal at the "Sum In" input produces an output equal to the amplitude setting. To maintain linearity, the sum of the internal waveform and the "Sum In" waveform should not exceed the amplitude setting. In equation form:

$$(W \div 2047) + (S \div 5) \leqslant 1$$

where W is the internal digital data (Y) value and S is the voltage at the "Sum In" input at any time. Because of this, attention needs to be given to the output voltage at the break point location at the end of each waveform.

3.25 PARALLEL OPERATION

Several Model 75's can be connected in parallel (as shown in the following diagram) to produce simultaneous waveforms (see figure 3-5) with a controllable phase relationship.



To connect Model 75's in parallel, chose one as the frequency master and connect its "Ref Out" to the "Ref In" inputs of the other Model 75's. The master should be set to internal reference and the others set to external reference. Starting with the master unit, the "Sync Out" output of each unit should be connected to the "Sync In" input of its successor.

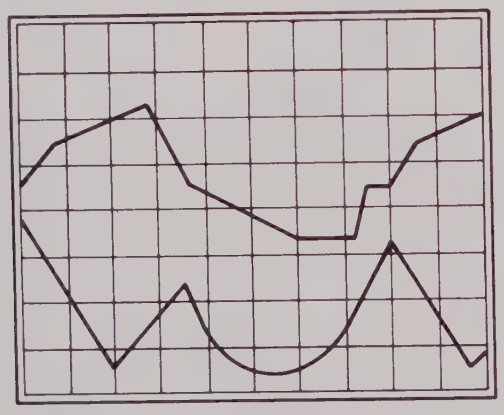


Figure 3-5. Example of Parallel Waveform

The position of the "Sync Out" pulse from one Model 75 controls the phase of the following Model 75. There are two ways of adjusting the position of the "Sync Out" pulse. One is to use the "SYNC" soft key from the "Set Up" menu to adjust the position by the actual address or phase of the pulse itself. The other is to use the "PHASE" soft key from the Set Up menu to adjust the phase relationship of the successive Model 75's in degrees. The difference between the two soft keys is due to the fact that there is a two clock cycle phase delay from a pulse in at the "Sync In" input to the start address output level at the output.

After initial setup and after any sync position change, each instrument must output a sync pulse before all of the phases will be synchronized. If the test setup uses a mode other than continuous, the outputs should be disconnected, and the Model 75's run momentarily in continuous mode to resynchronize the phase after a phase change.

3.26 GPIB CONTROLS (Option 001 Only)

The following paragraphs are keyed to controls in figure 3-6.

3.26.1 GPIB Address DIP Switches (6)

At power on, the bit address DIP switch (located on a PC Board under the top cover) selects the GPIB default ADRS (address) value. This value may be changed from the front panel. At power off the address returns to the bit switch setting. See paragraph 2.2.6 bit switch settings.

3.26.2 Setup Menu Key (4)

Pressing this key five times enables the GPIB communication soft keys described below. The bottom line of the display will then show the labels for these soft keys.

3.26.3 BUFFR Soft Key (3)

For remotely operated units the BUFFR soft key (from the SETUP menu) will display the last 16 ASCII characters received by the GPIB interface. Rotating the Control knob will scroll through the last 80 ASCII characters received by the GPIB interface. This feature can be used as a debugging tool for remote instrument programming.

3.26.4 ADRS Soft Key (2)

Pressing this key (from the SETUP menu) allows the user to manually set the GPIB address to some value other than that set by the internal DIP switches.

3.26.5 LOCAL Soft Key (1)

Pressing this key (from the SETUP menu) brings the Model 75 into local control providing the controller has not locked out the key (see paragraph 3.28.1).

3.26.6 Control Knob (5)

Allows the user to scroll through the ASCII characters received on the GPIB bus when the BUFFR soft key has been pressed or to set the GPIB address when the ADRS soft key is pressed.

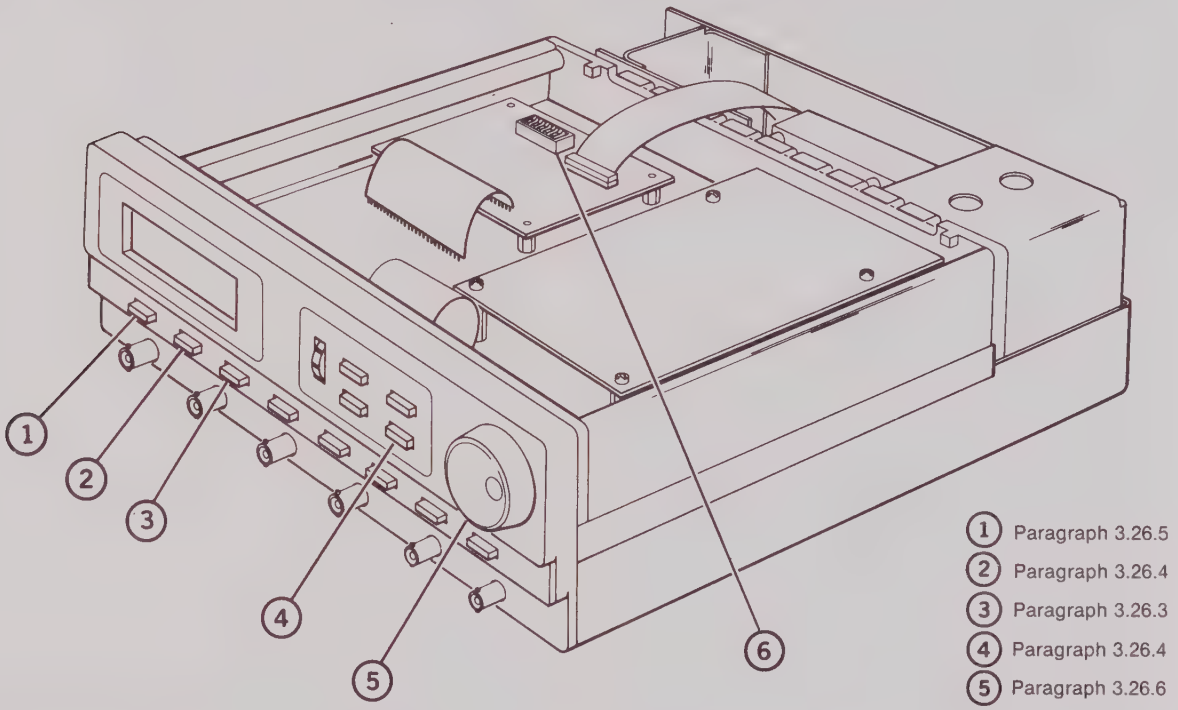


Figure 3-6. GPIB Controls and Switches

3.27 GENERAL PURPOSE INTERFACE BUS (GPIB)

Paragraphs 3.27 through 3.27.9 are provided for readers who wish further background information on the General Purpose Interface Bus (GPIB). For specific Model 75 programming information, refer to paragraph 3.28 through 3.29.3.

The GPIB interface is an implementation of IEEE specification 488-1978. It supports the following interface functions which are described in detail in the specification. Relevant aspects of these functions are discussed in following paragraphs.

SH1	Complete source handshake.
AH1	Complete acceptor handshake.
T6	Basic talker.
TE0	No extended talker.
L4	Basic listener.
SR1	Complete service request (software select).
RL1	Remote/local and local lockout.
PP0	No parallel poll capability.
DC1	Complete device clear/selective device clear.
DT1	Complete device trigger capability.
E1	Open collector drivers.

Instruments on the bus may have "talk" and "listen" capabilities. The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

The GPIB consists of 16 negative true signal lines as shown in figure 3-7. These 16 lines include 8 bidirectional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull up and active pull down. Thus, any device may "assert" a line by pulling it down to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

As shown in figure 3-7, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. The Model 75 is both a talker and a listener. More than one controller may be connected to the bus, but only one controller may be hard wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

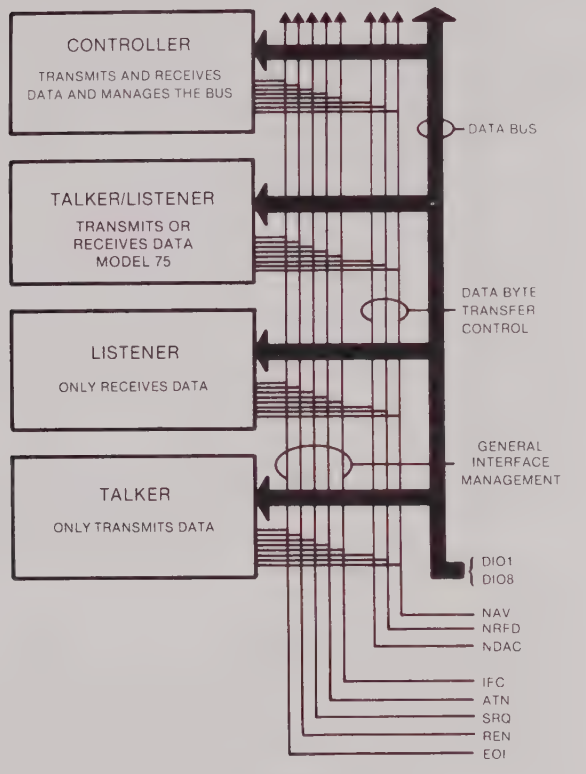


Figure 3-7. GPIB Structure

3.27.1 Bus Line Definitions

The 16 negative-true GPIB signal lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Valid
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

The functions of the GPIB signal lines are:

DIO1-DIO8 — These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN — The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller originated messages.

REN — The Remote Enable line controls whether devices on the GPIB are in local or remote modes. In the local mode, devices respond to front panel commands. In remote mode, the situation is reversed; GPIB originated commands are obeyed, while front panel commands are ignored. The Wavetek Model 75 enters the remote state when it receives its listen address and REN is enabled. The Wavetek Model 75 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LOCAL front panel soft key is pressed.

DAV, NRFD, NDAC — These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information.

EOI — When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the Wavetek Model 75 receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When the Wavetek Model 75 transmits the last byte of a message (which is always a terminator character) it also sets EOI true.

SRQ — The Service Request line is used by the Wavetek Model 75 and other devices on the bus to signal the controller that they request attention. Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.

IFC — The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.27.2 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as described in the next paragraph.

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.27.3 Commands

Commands are sent over lines DIO1-DIO8 with ATN true. They are divided into five classes:

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands
   - DCL Device Clear
   - SPE Serial Poll Enable
   - SPD Serial Poll Disable
   - LLO Local Lockout
5. Addressed Commands
   - GTL Go To Local
   - SDC Selective Device Clear
   - GET Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A.

3.27.4 Listen Address

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes SP through >). A 32nd address, called unlisten (hexadecimal "3F", ASCII "?") is used to command all devices to not read data bytes. The low order five bits of Model 75 listen address is selected by internal DIP switches (see paragraph 2.2.6) or by the ADRS soft key. To temporarily change the GPIB address, press the ADRS soft key and turn the Control knob until the desired address is displayed. At power on, the address always matches the internal switches.

3.27.5 Talk Address

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 40 through 5E, ASCII codes @ through). A 32nd address, called untalk (hexadecimal 5F, ASCII "_") is used to command all devices to cease talking. The low order five bits of the Model 75 talk address will be the same as the low order five bits of the listen address. Thus, if the Model 75 listen address is hexadecimal 21 (ASCII "!"), the talk address is hexadecimal 41 (ASCII "A").

3.27.6 Secondary Address

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the Model 75.

3.27.7 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Model 75 are:

1. Device Clear (DCL) — Resets the Model 75 to the default settings. DCL affects all devices on the bus.

2. Serial Poll Enable (SPE) — Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to all zeros, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the Model 75 talk message number 1. When this message is read, the status byte is reset and the SRQ released as for the serial poll.

3. Serial Poll Disable (SPD) — Discontinues serial poll. Returns instrument to normal talk modes.

4. Local Lockout (LLO) — Causes the Model 75 to enter a state where the front panel LOCAL soft key is inoperative. In this state the instrument will only accept parameter changes through the GPIB. To enable front panel parameter changes, the GPIB controller can send the GTL (Go To Local) command.

3.27.8 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the Model 75 are:

1. Go To Local (GTL) — Commands the Model 75 to go to the local mode.
2. Selective Device Clear (SDC) — Resets the Model 75 to its default conditions.
3. Group Execute Trigger (GET) — Upon receipt of the GET, the programmed settings are error checked. If no error is detected, the control information is transferred to the waveform generator circuit, followed by a trigger. In order to ensure system synchronization with a GET, the Model 75 will not complete the handshake sequence until it has finished execution of the GET.

3.27.9 Data Transfer

In addition to accepting programming characters, the Model 75 will transmit status and waveform information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument accepts the data as fast as possible (at approximately 120μs/character), until either 64 characters are received or there is a pause during the transfer of data. At the time, the entire string of received characters is scanned by the Model 75, which carries out the scan and accepts the next 64 character string. Whenever the Model 75 is finished scanning a string, the display will show the last parameter of the string and the current status of the GPIB interface. If the EOI line is asserted while sending a character to the Model 75, the currently programmed terminator character will be put into the input string following the character with the EOI.

3.28 MODEL 75 GPIB PROGRAMMING

This section describes the remote operation of the Model 75. For general GPIB programming information, refer to paragraph 3.27.

Paragraphs 3.28.1 through 3.28.5 provide background information and should be read before attempting to program the Model 75. Table 3-2 is a programming reference guide giving detailed descriptions of each programming character and information for writing actual statements to the Model 75.

3.28.1 General Programming Information

When the Model 75 is in remote mode, the menu and soft keys can still be used to examine the instrument settings, but the control knob will be inoperative so no settings can be changed. However, the real time keys (Trigger, Hold, Return) and the Counter key will function just as in local mode. When the instrument is in the remote mode, the GPIB interface input has priority over any front panel control, and the Control knob is completely ignored. Therefore, as long as the GPIB interface is continuously supplied with data, the keyboard will appear to be inoperative to the user.

Line 2 of the LCD always shows the state of the GPIB interface after scanning the last string (see paragraph 3.28.9). In the lower right corner, several characters may appear:

'R' = Remote
'L' = Addressed to listen
'T' = Addressed to talk
'Q' = Request of service because of selected SRQ mode

Line 1 is the parameter and special message readout. An asterisk (*) to the left of the parameter indicates that an execute has not been sent.

The front panel display is externally programmed by sending any ASCII character between single or double quotes, such as 'test string' or ''test string''.

The Model 75 is programmed by sending ASCII coded characters to the instrument (see table 3-2 and Appendix A).

3.28.2 Characters

There are 5 types of characters that can be sent over the GPIB bus. These are:

1. Alphabetic characters — 'A' through 'Z' (except 'E'). These select action or parameter commands. Both upper and lower case characters are accepted.
2. Numeric characters (Suffix) — These are '0' through '9', 'E' (exponent), '−' (negative), '+' (positive), and the decimal point. They control the selected parameter.
3. Special characters; The instrument will display any set of characters within single or double quotes, such as 'string'. The pound sign (#) initiates high speed data transfer (see paragraph 3.28.7).
4. Terminator — Designates the end of a character string. Initially, this is line feed (LF).
5. Nonprogramming characters — These are characters not in one of the previous described classes. They have no effect on programming and may be interspersed freely after any programming character other than 'X'.

3.28.3 Action and Parameter Commands

The alphabetic characters are used to select either actions or parameters. Nine characters select action commands. These cause an immediate action when sent and do not require entry of a numeric suffix. The remaining alphabetic characters are parameter commands and require one or two letters plus a numeric suffix to control some aspect of the instruments operation.

3.28.4 Action Commands

Action commands which cause an immediate action when sent and do not require entry of a numeric suffix are:

'J' (Manual trigger asserted)
'H' (Manual trigger unasserted)
'I' (Execute)
'Z' (Reset)
'Y' (Clear all break points)
'G' (Return)
'XC' (Display counter)
'XH0' (Hold Off)
'XH1' (Hold On)

To program an action, simply send the proper character to the GPIB interface. For example, to reset the Model 75, simply send the letter 'Z'. The action will then take place, but only if the instrument is in the remote state when the character is received by the instrument. See paragraph 3.28.1 REN (Remote Enable) for further information.

3.28.5 Programming Parameters

Parameter commands require one or two letters plus a numeric suffix to control some aspect of the instrument's operation.

There are only two exponent digits allowed. Only one decimal point and one 'E' (exponent) are allowed per number, all others are ignored. Any number of non-programming characters may be interspersed with the numeric suffix as they have no effect.

To examine the current value of a parameter, simply send the proper alphabetic character (F = frequency etc.).

To change a parameter value, first send the alphabetic character which selects the desired parameter. Next, send the new value using numeric characters ('0' through '9', 'E', '−', '+', and '.'). Data entry can be fixed point, floating point, exponential notation or scientific notation. Any sequence of characters which gives the new value is acceptable. For example, all of the following sequences cause sample frequency 100 Hz to be programmed.

Programming string for Frequency 100 Hz	Remarks
F 10 0	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E−2−	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the number input format is so general, the instrument must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic character, a special character, or a terminator character. When this is done, the new value is rounded off and tested to see if it is a legal value for the setting being changed. If it is legal, the new value will then be entered into the instrument's scratchpad memory.

Many of the parameters are held in a scratchpad memory when received and do not actually change the instrument setup until an "I" (Execute) or a GET is received by the Model 75. This allows several parameters to be changed simultaneously. If the Model 75 has not received an "I", and the scratchpad value of the displayed parameter is different than the current instrument setup, an asterisk (*) is shown on the display (see paragraph 3.28.1). When an "I" or a GET is received, all of the parameters are checked for conflicts and if no error occurs, the scratchpad contents are transferred to the instrument setup. An execute (I) may be sent as the last character in the parameter string if the new parameter is to be changed immediately.

It is also possible to send multiple commands in the same string. For example, to change frequency, amplitude and offset simultaneously, send the parameter string: 'F1E4A2D1I'. In this example, the new frequency is 10 kHz, amplitude is 2 Vp and offset is 1V. Because an execute was sent at the end of this string, the parameter changes are executed immediately.

3.28.6 Sending Waveforms to the Model 75

Waveforms are sent to the Model 75 by sending a 'K' followed by a number representing the first address (X location) to be changed in the waveform, then sending successive data values (Y values) preceded by 'L's until

the end of the waveform. Each time an 'L' is sent followed by a Y value the waveform address is incremented. Sending a 'K' followed by an address only affects the transfer of waveform data and does not affect the waveform directly. Any part of the 8192 point waveform memory can be written to whether or not it is between the current start and stop addresses (active waveform). For example, sending a 10 step ramp from X = 20 to X = 29 would be accomplished by sending the following to the Model 75;

K20, L-2047, L-1592, L-1137, L-682, L-227, L227, L682, L1137, L1592, L2047.

3.28.7 High Speed Binary Waveform Transfer

With software versions 2.14 and later, waveform data can be sent to the Model 75 in binary form at a rate of approximately 14.5 kbytes/s (each waveform point takes 2 bytes) from a fast GPIB controller such as the Wavetek Model 6000. In this way a 2048 point waveform can be sent to the Model 75 in 280 ms. To check the software version number, press RSET from the Setup menu (do not press execute unless you want to reset the instrument) and read the top line of the display.

To send a block of waveform data, send an ASCII "#" ($23), then a 2 byte binary beginning address with the most significant byte (MSB) first, then a 2 byte binary word count (MSB first), then the two byte data words (MSB first). The beginning address and the word count must be less than 8192. The word count is the number of waveform data points to be changed and must exactly correspond to the number of data words. Each data word is a two byte binary word representing a number between 0 and 4095. The actual Y-value of each data point is 2048 less than the value of the data word. For example, a data word of 1 corresponds to as Y-value of −2047.

The Model 75 must be completely finished processing all previous commands and any numeric input must be terminated prior to receiving the "#" character. The best way to insure this is to send a terminator character (typically LF) and a GET to the Model 75 prior to the "#". If the trigger cannot be tolerated, be sure that the Model 75 has had enough time to processes all previous commands before sending the "#".

If the beginning address or the word count are outside the allowable range, or one half second elapses without receiving any data, the high speed transfer will be aborted. Any data received after this will be interpreted as ASCII characters and may cause the Model 75 to act unpredictably. Because of this low tolerance for errors, the high speed waveform transfer method should be used with extreme care.

3.28.8 Reading Waveforms From the Model 75

Reading waveform data from the Model 75 to a computer is accomplished by setting the talk mode to 7 by sending an 'XT7' and then reading successive data values (Y values) from the Model 75. Data values are read starting at a location specified by sending a 'K' followed by the address (X value) of the first point. Each time a data value is read, the waveform address is incremented. Neither sending a 'K' followed by an address nor reading a data value has any direct effect on the wavedform output.

3.28.9 Programming Reference Guide

Table 3-2 can be used as a programming reference guide when sending commands to the Model 75. It describes each programming character and which numeric characters are to be used to program parameter values. Before attempting to use this guide, read paragraphs 3.28.1 through 3.28.5.

When programming the Model 75, keep in mind that at initial power up, the following remote settings have been defaulted.

Function	ASCII Character	Default Setting
GPIB ADRS	—	Bit Switch
SRQ Mode	XQ	1
Talk Mode	XT	0
Terminator	XV	10

Table 3-2. Programming Reference Guide

Function	ASCII Character	Description
Sample Frequency	F*	The character 'F' followed by a number value programs the sample frequency in hertz. An 'E' designates exponent. Valid frequency values are 2E – 2 to 2E + 6. This is the same as the SAMPL soft key.
Amplitude	A*	The character 'A' followed by a number value programs the peak amplitude into the 50Ω impedance at the ARB Out connector. Valid amplitude values are 5E – 3 to 5.1. This is the same as the AMPL soft key.
Offset	D*	The character 'D' followed by a number value programs the offset voltage into 50 Ω at the ARB Out connector. Valid offset values are – 5.10 to + 5.10. This is the same as the OFFSET soft key.
Burst Count	U*	The character 'U' followed by a number value programs the number of cycles in the burst. The count number can be from 1 to 1,048,575 cycles. This is the same as the BURST soft key.
Start Address	T*	The character 'T' followed by a number programs the waveform start address. The valid start addresses are 0 to 8191. This has the same function as the START soft key.
Stop Address	P*	The character 'P' followed by a number programs the waveform stop address. The valid stop addresses are 0 to 8191. This has the same function as the STOP soft key.
Sync Address	S*	The character 'S' followed by a number programs the waveform SYNC address. The valid sync addresses are 0 to 8191. This has the same function as the sync soft key.
Ramp Rate	M*	The character 'M' followed by a number programs the ramp rate for the return feature. Valid range is 0 to 100 and represents ms/step. Same as the RAMP soft key.
ARB Address	K	The character 'K' followed by a number sets the waveform address for sending or receiving waveform data to or from the Model 75. This had no direct effect on waveform output. Valid range is 0 to 8191.
ARB Data	L	The character 'L' followed by a number sets one data point at the current waveform address and increments the address by one. Valid range is – 2047 to + 2047.
Calibration	N	The character 'N' followed by a number sets the offset calibration constant and should only be used for calibrating the instrument. Same as the CAL soft key. Valid range is – 512 to + 512.
Set Break Point	V	The character 'V' followed by a number sets a break point at the address specified by the number. Valid range is 0 to 8191.
Clear Brk Point	W	The character 'W' followed by a number clears the break point at the specified address. Valid range is 0 to 8191.

Table 3-2. Programming Reference Guide (Continued)

<table>
<tr><th>Function</th><th>ASCII Character</th><th>Description</th></tr>
<tr><td>Terminator Select</td><td>XV</td><td>When the power is turned on, the terminator or End Of String (EOS) character (see EOI description, paragraph 3.28.1) is the ASCII line feed 'LF'. If the GPIB controller does not look for the end message (EOI line low), and it does not recognize the line feed (LF) as a string terminator, a new EOS character will be needed. The EOS terminator may be changed to any ASCII character (except NUL) by sending 'XV' followed by the decimal value (of the ASCII code) corresponding to the new terminator.</td></tr>
<tr><td>Function</td><td>C</td><td>The character 'C' followed by a single digit code between 0 and 8 selects standard waveform which is inserted between start and stop addresses.

FUNCTION — CODE
Sine wave — C0
Triangle wave — C1
Square wave — C2
Ramp Up — C3
DC — C4
Ramp Down — C5
Cosine — C6
Inv Sine — C7
Haver Sine — C8</td></tr>
<tr><td>Mode</td><td>B*</td><td>The character 'B' followed by a single digit code between 0 and 4 selects the operating mode of the instrument.This is the same as the MODE soft key.

MODE — CODE
Continuous — B0
Triggered — B1
Gated — B2
Toggled — B3
Burst — B4</td></tr>
<tr><td>Trigger Slope</td><td>Q*</td><td>The character 'Q' selects generator triggering or gating on the rising or falling edge of the Trig In (TTL) signal or GPIB 'J' (positive slope) or 'H' (negative slope) command. See TRIGGERING/GATING CHART below.

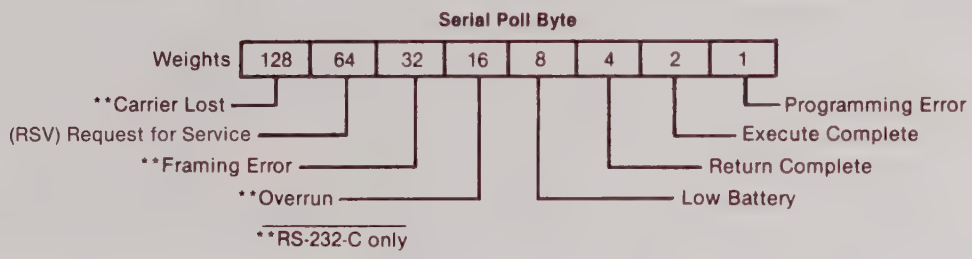
TRIGGERING/GATING CHART
<table><tr><th></th><th>Positive Slope (Rising Edge) Q0</th><th>Negative Slope (Falling Edge) Q1</th></tr><tr><td>'J'</td><td>Trig: Single cycle
Gate: Free runs
Toggle: Toggles
Burst: Start burst</td><td>Trig: Enable 'H'
Gate: Off
Toggle: Enable 'H'
Burst: Enable 'H'</td></tr><tr><td>'H'</td><td>Trig: Enable 'J'
Gate: Off
Toggle: Enable 'J'
Burst: Enable 'J'</td><td>Trig: Single cycle
Gate: Free runs
Toggle: Toggles
Burst: Starts Burst</td></tr></table></td></tr>
</table>

Table 3-2. Programming Reference Guide (Continued)

Function	ASCII Character	Description
Reference		Same as pressing the REF soft key. Allows the user to select either an external frequency reference or the internal reference using the 'R' parameter followed by a 0 or a 1.
Internal	R0*	Selects an internal source as the frequency reference.
External	R1*	Selects an external source as the frequency reference.
Execute	I	The character 'I' is an action command that causes all parameters in the scratchpad to be checked for conflicts. If no error is found, the rounded scratchpad contents are transferred to the instrument setup. An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.
Reset	Z	The character 'Z' is an action command that sets the instrument setup, waveform, and scratchpad memories to the defined default values.
Trigger		In remote operation, triggered, gated, toggled, and burst modes of the generator are initiated by an external signal at the Trig In connecter, the front panel trigger key or the 'J' and 'H' commands via the GPIB.
Man. Trig. Pressed	J	Turns trigger on (must be followed by an "H" to turn trigger off). See TRIGGERING/GATING CHART.
Man. Trig. Released	H	Turns trigger off (must be followed by an "J" to turn trigger on). See TRIGGERING/GATING CHART.
Hold Off	XH0	The characters 'XH' followed by a 0 will turn the hold circuitry off allowing the waveform to continue.
Hold On	XH1	The characters 'XH' followed by a 1 will turn the hold circuitry on causing the waveform to stop at its instantaneous value.
Return	G	The character 'G' causes the output to ramp back to the starting "Y" value. The rate of the ramp is adjustable from 0 to 100 ms per point. If the instrument is in Continuous mode, the output will be held after the return and can be restarted by pressing the Hold key or sending an XH0 over the GPIB bus. If the waveform is in the Trigger, Gate, Toggle, or Burst mode, the output will wait for another trigger (manual or external) before restarting. This is the same as the Return key.
Display Counter	XC	The characters 'XC' causes the waveform counter to displayed on the Model 75 display. Same as the COUNTER key.
Clear ALL Break Ponts	Y	The character 'Y' clears ALL breakpoints and inserts one at the start address. Same as the CLRBPS soft key.
SRQ Mode	XQ	The characters 'XQ' followed by a value ("0" to "255") selects the conditions under which the Model 75 asserts the SRQ line on the GPIB bus and sets the RSV bit in the serial poll response byte. The equivalent binary value is a "mask" for the serial poll response byte. All RS-232-C bits will have no effect if selected.

Table 3-2. Programming Reference Guide (Continued)

Function	ASCII Character	Description



SRQ Mode	XQ	Each bit enables the associated condition to cause a service request. Each condition may be enabled individually or in combination with others. The RSV bit is always enabled. Examples: 'XQ0' disables the SRQ line. 'XQ1' asserts the SRQ line and RSV bit when there is a program error such as "offset" beyond the Model 75 limits. 'XQ9' initiates a service request if either a program error has occurred or the battery voltage is detected low.
Number Character	0-9, E, +, −, and decimal.	The numeric characters '0' through '9', 'E', '+', '-', and decimal point are used to program new parameter values. Data entry is free format, i.e., fixed point, floating point and exponential notation, or scientific notation.
Talk Mode	XT	To read a message from the Model 75, send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Mode (XT) setting. The last character of the Model 75's message will be the currently programmed terminator character with the EOI line asserted. The characters 'XT' followed by a code (0 through 7) selects the kind of message the 75 will send when it is addressed as a talker on the GPIB. CODE MESSAGE XT0 Programming error list. A typical error string is E 1F 2AD. Some error string characteristics are: a. All error strings begin with 'E'. b. Most recent error is at the end of the string. c. Errors are separated by space. d. Class 1 error: The number "1" followed by the programming character that caused the error (example 1F). e. Class 2 errors: The number "2" followed by the two conflicting parameters. f. Class 3 errors: Start, stop, sync conflict. g. Error strings can be up to 80 characters in length. h. After transfer, the instrument clears the error string.

Table 3-2. Programming Reference Guide (Continued)

Function	ASCII Character	Description
		XT1 Poll Byte response: The byte (see paragraph 3.28.7) that is sent if a serial poll was performed. The controller, by reading this byte, causes the instrument to clear the poll byte and reset the SRQ line if asserted. The format is an ASCII "P" ($50) followed by an ASCII space ($20) followed by the poll byte.
		XT2 The most recently selected parameter and its value. Example: Freq 1.23E3. If no parameter is selected, the instrument returns NO PARAMETER SELECTED.
		XT3 The entire instrument setup after last execute. Example: A5 B0 D0 F1E6 P2047E3 Q0 R0 S0 T0 U8 XH0.
		XT4 The entire scratch pad instrument setup that will be entered when execute is received; same format as XT3.
		XT5 Instrument identification: Wavetek Model 75 V(X.Y). 'X.Y' identifies the software version number.
		XT6 Waveform counter value.
		XT7 Waveform data at the current waveform address, also causes the current address to be incremented.
Exponent	E	Causes the number preceding the "E" (mantissa) to be multiplied by 10 raised to the power of the number following the "E" (exponent). The exponent is limited to two digits and a + or − sign. For example F3E − 1 sets the frequency to 0.3 Hz.

*An asterisk (*) following the character in the "ASCII Character" column indicates that this command will not affect the actual instrument setup until an execute character (I) is received by the Model 75 (see paragraph 3.28.5).

3.29 ERRORS — GPIB REPORTING

When an illegal value is programmed or interdependent parameter errors are detected, an error signal is indicated by adding an error code to the error string and pulling the SRQ line low if the SRQ mode is an odd number. The controller can then serial poll the instruments to locate the source of the service request. It then inquires as to the nature of the request. The method of reporting errors on the GPIB is given in table 3-2 (SRQ Mode and TALK mode).

3.29.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the selected parameter. For example, programming an amplitude of 500 volts will cause a parameter error when the next alpha character is programmed. At this time, the Model 75 disregards the new value and retains the previously programmed value.

Example:

After receiving a frequency value, a round off is made followed by the limit test 20E − 3 to 2E + 6. Any value outside the boundaries listed in table 3-3 causes a class 1 error.

Table 3-3. Class 1 Error Guidelines

This Parameter	Must (After Rounding) Be
ARB Address	0 to 8191
ARB Data	−2047 to +2047
Amplitude	5E−3 to 5.1
Burst Count	1 to 1,048,575
Calibration	−512 to +512
Clear Breakpoint	0 to 8191
Hold	0 to 1
Mode	0 to 4
Offset	−5.1 to +5.1
Ramp Rate	0 to 100
Ref	0 to 1
SRQ Mode	0 to 255
Sample Frequency	20E−3 to 2E+6
Set Breakpoint	0 to 8191
Standard Waveform	0 to 8
Start Address	0 to 8191
Stop Address	0 to 8191
Sync Address	0 to 8191
Talk Message	0 to 7
Terminator	0 to 127
Trigger Slope	0 to 1

3.29.2 Class 2 Errors

Class 2 errors are parameter conflicts or inconsistencies such as ABS(OFST) + peak amplitude greater than 5.2V. Tests are made every time an execute (I) is given. If no class 2 error is detected, all scratchpad values are transferred to the instrument setup.

3.29.3 Class 3 Errors

A class 3 error is a parameter conflict or inconsistency between the Start Address, Stop Address, and Sync Address parameters. Tests are made every time an execute (I) is given. If no class 3 error is detected, all scratchpad values are transferred to the instrument setup.

3.30 RS-232-C CONTROLS

The RS-232-C controls listed in paragraphs 3.30.1 thru 3.30.6 are referenced to figure 3-8, RS-232-C Controls and Switches.

3.30.1 Setup Menu Key (4)

Pressing this key five times enables the RS-232-C communication soft keys described below. The bottom line of the display will then show the labels for these soft keys.

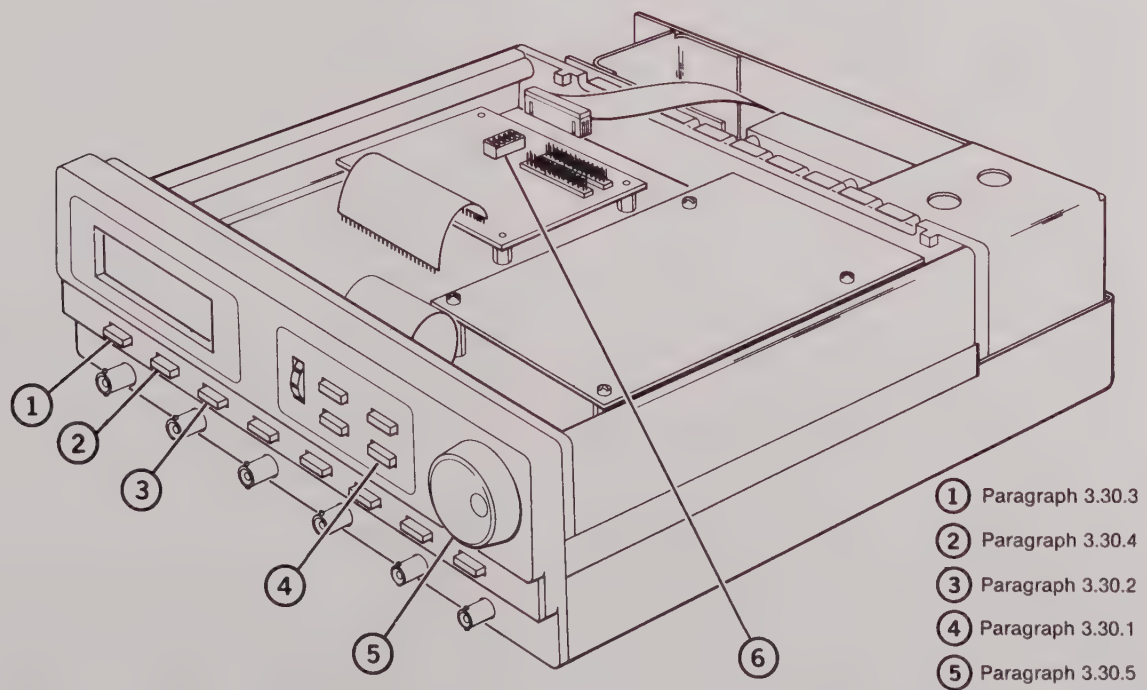


Figure 3-8. RS-232-C Controls and Switches

3.30.2 BUFFR Soft Key (3)

For remotely operated units the BUFFR soft key will display the last 16 ASCII characters received by the serial interface. Rotating the Control knob will scroll through the last 80 ASCII characters received by the RS-232-C interface. This feature can be used as a debugging tool for remote instrument programming.

3.30.3 LOCAL Soft Key (1)

Pressing this soft key from the SETUP menu brings the Model 75 into local control providing that the controller has not locked out the key (with the '*' character).

3.30.4 HAND Soft Key (2)

Pressing the HAND soft key (2) from the SETUP menu allows the user to change the handshake mode from XON/XOFF to CTS/DTR or vice versa by rotating the Control knob (5).

3.30.5 Control Knob (5)

Allows the user to scroll through the ASCII characters received over the serial interface bus when the BUFFR soft key has been pressed. It also changes the handshake from CTS/DTR to XON/XOFF when the HAND soft key is pressed.

3.30.6 Baud Rate Switch (6)

Changing the position of each individual switch section (and therefore the overall combination) in the Baud Rate switch produces a different baud rate for the serial port. See Section 2.2.8.

3.31 GENERAL RS-232-C INFORMATION

EIA standard RS-232-C specifies the electrical characteristics and pin out of a serial communication standard for connecting "data terminal equipment" (DTE) to "data communication equipment" (DCE). Data terminal equipment is usually devices such as terminals, computers, or printers that are the final destination for data. Data communication equipment, on the other hand, is usually a modem or other device that converts the data to another form and passes it through. Because RS-232-C signal lines defined as inputs on a DCE device are outputs on a DTE device and vise versa, connection of a DCE to another DCE or of a DTE to another DTE will require a special cable with many of the signals interchanged. These cables are often called "modem eliminators" because they are used to eliminate a pair of modems between two computers. The Model 75 can be configured as either a DCE or DTE device, so in most cases it can be connected with a straight through cable to either a computer or to a modem.

The baud rate is the bit rate during the transmission of a word in bits per second. Different devices use many baud rates but the baud rates of the two devices that are connected must be the same. The Model 75 can be set to 14 different baud rates ranging from 50 to 19,200 as described in paragraph 2.2.8 and table 2-4.

Data signals over the RS-232-C use a voltage of +3 to +25V to represent a zero (also called a space) and a voltage of −3 to −25V to represent a one (also called a mark). Handshake and control lines use +3 to +25V to indicate a true condition and −3 to −25V to indicate a false condition.

When no data is being transmitted, the idle state of the data lines will be the mark state. To transmit a byte, the transmitting device first sends a start bit which is a space for one bit time (1/baud rate) to synchronize the receiver. Next, the data bits are sent LSB first (the Model 75 uses 8 data bits), then at least one bit time of the mark state (stop bits) before initiating the transmission of the next byte. Some devices use an optional parity bit between the data bits and the stop bits. The Model 75 does not support this and it should be suppressed on the connected device (see figure 3-9).

The RS-232-C standard is not very specific about many of the handshaking signals and it is therefore usually necessary to refer to the manuals for both of the devices being connected to determine the exact pin out, signal definition, and signal direction for the devices (see paragraph 2.2.7, 2.2.8, and table 2-3) for the Model 75 pin outs).

Handshaking is used so that each device can tell the other device when it is ready or not ready to receive data. The Model 75 supports two different types of handshaking, CTS/DTR (hardware handshaking) and XON/XOFF (see table 3-4). With hardware handshaking, the DCE device pulls the CTS line positive or negative to indicate whether it is ready or not ready respectively and the DTE device pulls the DTR line positive or negative to indicate whether it is ready or not ready respectively. With XON/XOFF handshaking either device sends an XOFF ($13) over the appropriate data line when it is no longer ready to receive data, then sends an XON ($11) when it is again ready.

When the Model 75's DTR (DCE configuration) or CTS (DTE configuration) line is pulled negative, it will send a maximum of one character before it stops transmitting and waits for the handshake line to return positive. When the Model 75 receives an XOFF character it will send a maximum of 3 characters before it stops transmitting and waits to receive an XON character.

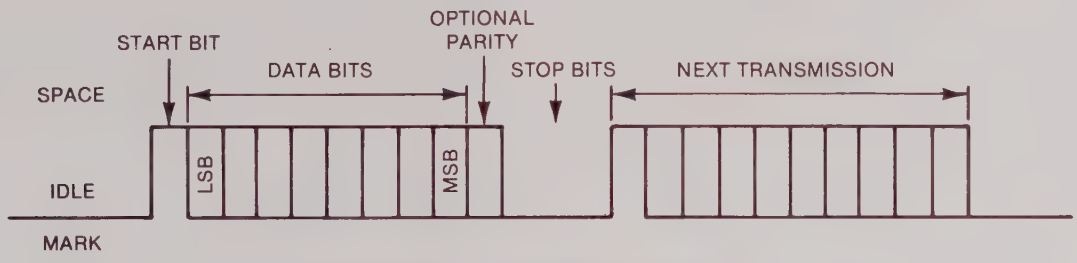


Figure 3-9. Transmission Example

When the Model 75's internal buffer fills, it will do one of two things depending on the handshaking mode set from the HAND soft key. If the handshaking mode is CTS/DTR, the Model 75 will set the CTS line negative if it in the DCE configuration or set the DTR line negative if it is in the DTE configuration. When the Model 75 is again ready to receive data it will set the appropriate line back positive. If the handshaking mode is set to XON/XOFF, the Model 75 will send an XOFF character over the data line. When it is again ready to receive data it will send an XON. After the Model 75 either sets the handshake line negative or sends the XOFF, the connected device must stop sending data within 10 characters or data will be lost.

The SRQ mode (XQn) has no effect over the RS-232-C interface, however the serial poll byte can be read using talk mode (XT1). The bits of the serial poll byte are defined in the same way as over the IEEE-488 interface and all bits are always enabled.

When the instrument is in the remote mode (sending the character '!' causes the instrument to go to remote), the RS-232-C interface input has priority over any front panel control, and the Control knob is completely ignored. Therefore, as long as the serial interface is continuously supplied with data, the keyboard will appear to be inoperative to the user.

Line 2 of the LCD always shows the state of the serial interface after scanning the last string. In the lower right corner, a character will appear:

'R' = Remote (if the unit is in remote)

Line 1 is the parameter and special message readout. An asterisk to the left of the parameter indicates that an execute has not been sent.

The front panel display is externally programmed by sending any ASCII character between single or double quotes, such as 'test string' or "test string".

The Model 75 is programmed by sending ASCII coded characters to the instrument (see table 3-2 and Appendix A).

3.31.1 Characters

There are 6 types of characters that can be sent over the RS-232-C interface. These are:

Alphabetic characters; 'A' through 'Z' (except 'E'). These select action or parameter commands. Both upper and lower case characters are accepted.

Numeric characters (Suffix); These are '0' through '9', 'E' (exponent), ' − ' (negative), ' + ' (positive), and the decimal point. They control the selected parameter.

Special characters; The instrument will display any set of characters within single quotes, such as 'string'.

Interface Control Characters; These are the characters '!', '*', '$', '?', 'XON', and 'XOFF'.

Terminator; Designates the end of a character string. Initially, the instrument will accept a 'CR' or a 'LF' and send a 'CR + LF' as a terminator.

Nonprogramming characters; These are characters not in one of the previous described classes. They have no effect on programming and may be interspersed freely after any programming character other than 'X'.

3.31.2 RS-232-C Terminators

Upon "power-on", the Model 75 accepts either a carriage return (CR) or a line feed (LF) as an end of string (EOS) terminator and sends both a CR and LF as the EOS terminator. If the connected device does not recognize either one, the terminator will need to be changed. The terminator can be changed to any ASCII character other than XON and XOFF, or NULL by sending 'XV' followed by the decimal ASCII code for the character. A terminator code of '0' is a special case and represents the default condition of sending a CR and LF and accepting either CR or LF as previously mentioned.

3.31.3 Action and Parameter Commands

The alphabetic characters are used to select either actions or parameters. Nine characters select action commands. These cause an immediate action when sent and do not require entry of a numeric suffix. The remaining alphabetic characters are parameter commands and require one or two letters plus a numeric suffix to control some aspect of the instruments operation.

3.31.4 Action Commands

Action commands which cause an immediate action when sent and do not require entry of a numeric suffix are:

'J' (Manual trigger asserted)
'H' (Manual trigger unasserted)
'I' (Execute)
'Z' (Reset)
'Y' (Clear all break points)
'G' (Return)
'XC' (Display counter)
'XH0' (Hold Off)
'XH1' (Hold On)

To program an action, simply send the proper alphabetic character to the RS-232-C interface. For example, to reset the Model 75, simply send the letter 'Z'. The action will then take place, but only if the instrument is in the remote state when the character is received by the instrument. See table 3.4 for further information.

3.31.5 Programming Parameters

Parameter commands require one or two letters plus a numeric suffix to control some aspect of the instrument's operation.

There are only two exponent digits allowed. Only one decimal point and one 'E' (exponent) are allowed per number, all others are ignored. Any number of non-programming characters may be interspersed with the numeric suffix as they have no effect (except for the interface control characters).

To examine the current value of a parameter, simply program the proper alphabetic character ('F' = frequency etc.).

To change a parameter value, first send the alphabetic character which selects the desired parameter. Next, send the new value using numeric characters ('0' through '9', 'E', '+', '−', and '.'). Data entry can be fixed point, floating point, exponential notation or scientific notation. Any sequence of characters which gives the new value is acceptable. For example, all of the following sequences cause sample frequency 100 Hz to be programmed.

Programming String for Frequency 100Hz	Remarks
F 100	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E-2-	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the number input format is so general, the instrument must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic character, a special character, or a terminator character. When this is done, the new value is rounded off and tested to see if it is a legal value for the setting being changed. If it is legal, the new value will then be entered into the instrument's scratchpad memory or executed immediately if an "I" is not required.

Some parameters require that they be followed by an execute (I). If an execute (I) has not been sent and the new value is different from the parameter in the scratchpad memory, an asterisk (*) is shown on the display. After an 'I' (execute) is sent, all the parameters in the scratchpad are checked for conflicts and if no error occurs the scratchpad contents are transferred to the instrument setup. An execute (I) may be sent as the last character in the parameter string if the new parameter is to be executed immediately.

It is also possible to send multiple commands in the same string. For example, to change frequency, amplitude and offset simultaneously, send the parameter string: 'F1E4A2D1I'. In this example, the new frequency is 10 kHz, amplitude is 2 Vp and offset is 1V. Because an execute was sent at the end of this string, the parameter changes are executed immediately.

3.31.6 Sending Waveforms to the Model 75

Waveforms are sent to the Model 75 by sending a 'K' followed be a number representing the first address (X location) in the waveform, then sending successive data values (Y values) preceded by 'L's until the end of the waveform. Each time an 'L' is sent followed by a Y value the waveform address is incremented. Sending a 'K' followed by an address only affects the transfer of waveform data and does not affect the waveform directly. Any part of the 8192 point waveform memory can be written to whether or not it is between the current start and stop addresses (active waveform). For example, sending a 10 step ramp from X = 20 to X = 29 would be accomplished by sending the following to the Model 75;

K20, L-2047, L-1592, L-1137, L-682, L-227, L227, L682, L1137, L1592, L2047.

3.31.7 Reading Waveforms From the Model 75

Reading waveform data from the Model 75 to a computer is accomplished by setting the talk mode to 7 by sending an 'XT7' and then reading successive data values (Y values) from the Model 75. Data values are read starting at a location specified by sending a 'K' followed by the address (X value) of the first point. Each time a data value is read, the waveform address is incremented. Neither sending a 'K' followed by an address nor reading a data value has any direct effect on the waveform output. To read a data value over the RS-232-C interface, send a '?' to cause the Model 75 to send the data value.

3.31.8 Programming Reference Guide

Except for "XV" (terminator), table 3-2 in the GPIB section applies to the RS-232-C interface as well as the GPIB bus and can be used as a reference guide when sending commands to the Model 75. It describes each programming character and which numeric characters are to be used to program parameter values.

When programming the Model 75, keep in mind that at initial power-up, the following remote settings have been defaulted.

Function	ASCII Character	Default Setting
Talk Mode	XT	0
Terminator	XV	0 (Accept a CR or LF and send a CR + LF.)

Table 3-4. RS-232-C Interface Control Commands

Character	ASCII	Function
!	$21	Causes the Model 75 to go into remote mode. In remote mode the instrument setup can only be changed from the RS-232-C interface and not from the front panel. The front panel keys will still be active and can be used to query the instrument setup conditions. The instrument can be returned back to local mode by sending a '$' over the interface or pressing the LOCAL soft key (unless it locked out by '*', see below).
$	$24	Causes the Model 75 to go to local mode. In local mode the instrument setup can be changed only from the front panel and will ignore any commands from the interface (except '!').
*	$2A	Causes the Model 75 to disable the LOCAL soft key. After this, the only way the instrument can return to local mode is with a '$' character from the interface.
?	$3F	Causes the Model 75 to send the talk message as set by the talk mode (XTn) to the connected device.
XOFF	$13	Causes the Model 75 to stop transmitting data to the connected device (see handshaking above).
XON	$11	Cancels the XOFF condition allowing the Model 75 to continue transmitting.

3.32 ERRORS — RS-232-C REPORTING

3.32.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the selected parameter. For example, programming an amplitude of 500 volts will

cause a parameter error when the next alpha character is programmed. At this time, the Model 75 disregards the new value and retains the previously programmed value.

Example:

After receiving a frequency value, a round off is made followed by the limit test 20E-3 to 2E6. Any value outside the boundaries listed in table 3-5 causes a class 1 error.

Table 3-5. Class 1 Error Guidelines

This Parameter	Must (After Rounding) Be
ARB Address	0 to 8191
ARB Data	−2047 to +2047
Amplitude	5E-3 to 5.1
Burst Count	1 to 1,048,575
Calibration	−512 to +512
Clear Breakpoint	0 to 8191
Hold	0 to 1
Mode	0 to 4
Offset	−5.1 to +5.1
Ramp Rate	0 to 100
Ref	0 to 1
SRQ Mode	0 to 255
Sample Frequency	20E-3 to 2E6

Table 3-5. Class 1 Error Guidelines (Continued)

This Parameter	Must (After Rounding) Be
Set Breakpoint	0 to 8191
Standard Waveform	0 to 8
Start Address	0 to 8191
Stop Address	0 to 8191
Sync Address	0 to 8191
Talk Message	0 to 7
Terminator	0 to 127
Trigger Slope	0 to 1

3.32.2 Class 2 Errors

Class 2 errors are parameter conflicts or inconsistencies such as ABS (OFST) + peak amplitude greater than 5.2V. Tests are made every time an execute (I) is given. If no class 2 error is detected, all scratchpad values are transferred to the instrument setup.

3.32.3 Class 3 Errors

A class 3 error is a parameter conflict or inconsistency between the Start Address, Stop Address, and Sync Address parameters. Tests are made every time an execute (I) is given. If no class 3 error is detected, all scratchpad values are transferred to the instrument setup.

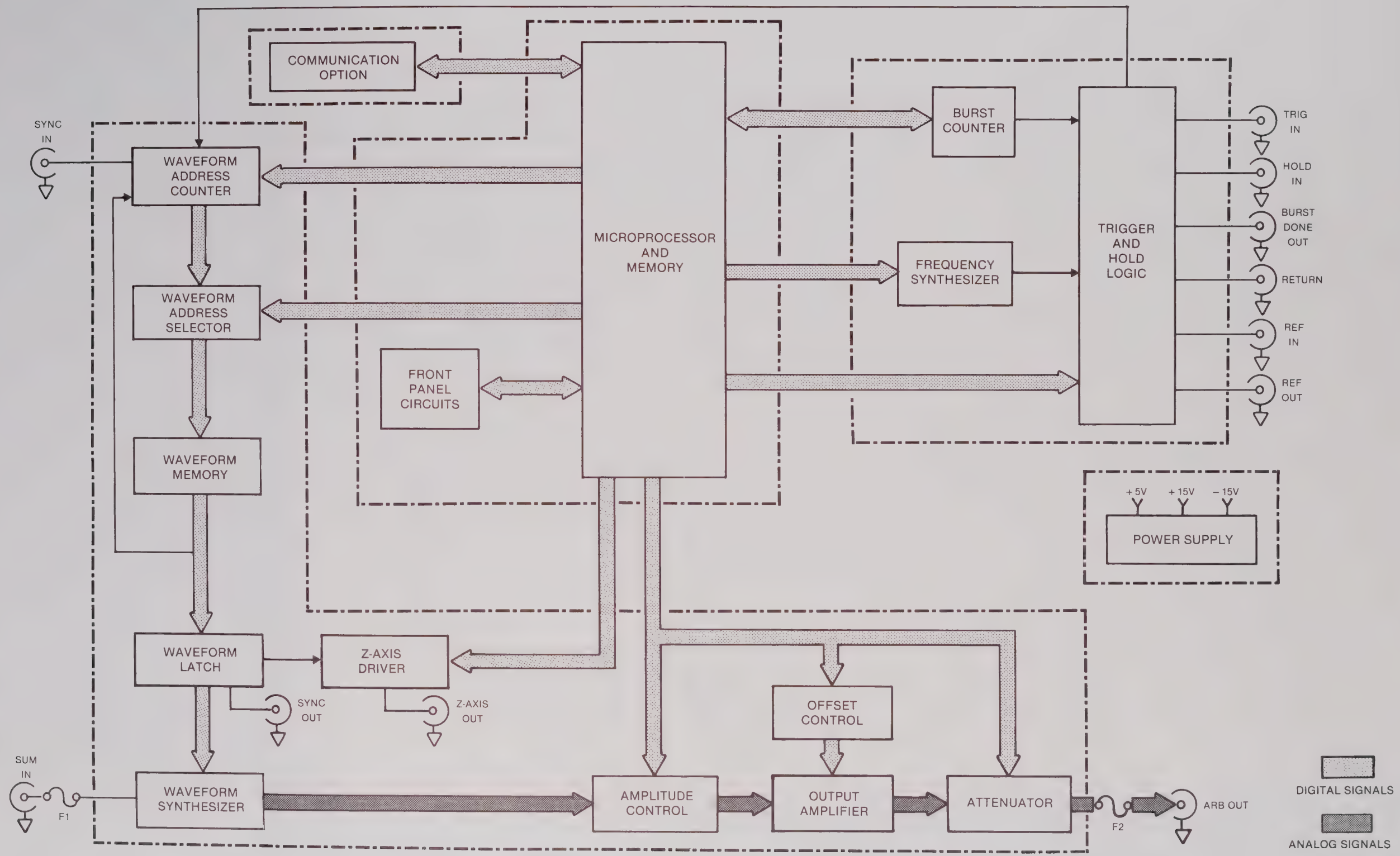


Figure 4-1. Model 75 Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The purpose of this section is to familiarize the user or service personnel with the circuit level operation of the Model 75. This knowledge is necessary to aid in troubleshooting of an instrument failure and may also allow the user to gain greater insight into the Model 75's versatility for particular applications.

The block diagram of the Model 75 is shown in figure 4-1. This block diagram is grouped into 5 functional blocks:

- **Signal Path** consisting of the waveform address counter, waveform address selector, waveform memory, waveform latch, waveform synthesizer, amplitude and offset controls, output amplifier, output attenuator, and Z-Axis driver.
- **Timing and Triggering** consisting of the frequency synthesizer, trigger and hold logic, and the burst counter.
- **Instrument Control** consisting of the microprocessor and memory section, and the front panel.
- **Communication Option,** if any installed, consisting of either an IEEE-488 card or an RS-232-C card.
- **Power Supply**.

Refer to figure 6-1, Troubleshooting Block Diagram, for a more detailed look at circuit block interaction.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Signal Path

4.2.1.1 General Description

The waveform memory contains the digital waveform data that originates from the microprocessor. The information to be accessed is determined by the waveform address counter which is updated at a rate determined by the Timing and Triggering section. The digital waveform information is sent through the waveform latch to the waveform synthesizer which converts it to an analog waveform. Any external signal applied to the Sum In input is summed together with the internal waveform at this point. The waveform is then run through the amplitude control. This circuit controls the amplitude within a 10 to 1 range based on data provided by the microprocessor. The offset control converts the digital information from the microprocessor to an analog voltage and applies that voltage to the output amplifier. The output amplifier sums the waveform and offset voltages and provides the final waveform amplification. The output attenuator controls the waveform amplitude in 3 single decade steps and maintains the 50 ohm output impedance.

4.2.1.2 Waveform Address Counter

Refer to schematic 0103-00-1389, sheet 3. The waveform address counter consists of four cascaded 4 bit binary counters (U24, U25, U28 and U36). The binary output of these counters provides the address, to the waveform memory, of the digital waveform information to be accessed. U24 pin 14 is the least significant address bit and U36 pin 14 is the most significant. The waveform start address, as set by the user, is applied by the microprocessor to the preload inputs of the counters (STRT12-STRT0). This address will appear on the outputs of the counters when pin 9 ($\overline{\text{LOAD}}$) is pulled low by the logic of U4C, U10C and U35C. When pin 9 ($\overline{\text{LOAD}}$) of the counters is released, the data on the counter outputs will increment by one with every rising edge on pin 2 (CLK). The CLK line originates in the Timing and Triggering section and its frequency is set by the user as sample frequency. When U24 counts from the binary number set by its preload inputs to binary 1111, U24 pin 15 (Ripple Carry Out) goes high and enables U25 for 1 count. This sequence repeats until U25 has counted to binary 1111, when its ripple carry out will go high enabling U28 for one count. The sequential counting will continue until an address is accessed where the $\overline{\text{LOAD}}$ bit (U11 pin 15) has been asserted. The $\overline{\text{LOAD}}$ bit is asserted in the waveform memory by the microprocessor at the address defined by the user as the waveform stop address. When $\overline{\text{LOAD}}$ goes low, pin 9 ($\overline{\text{LOAD}}$) of the counters is pulled low by U4C. This restarts the address counters at the start address and therefore restarts the waveform. An external sync pulse, applied to the Sync In input will also restart the waveform in the same

manner. The $\overline{\text{PLOAD}}$ input to U10C is used by the microprocessor to force the waveform memory to a specific address during a return to start. The NO LOAD input to U35C originates from the waveform memory control circuitry. Whenever the microprocessor reads from or writes to the waveform memory, NO LOAD goes high and blocks the reloading of the address counters. This prevents accidental restarting of the waveform if $\overline{\text{LOAD}}$ is pulled low during the microprocessor's access of the waveform memory. All locations in the unused portions of the waveform memory have $\overline{\text{LOAD}}$ asserted. This ensures that the waveform will restart even if the microprocessor is accessing the waveform memory when the stop address occurs.

4.2.1.3 Waveform Address Selector

Refer to schematic 0103-00-1389, sheet 3. The waveform address selector consists of four quad 2-input data selectors (U29, U19, U18 and U23). These data selectors determine whether the location in the waveform memory to be accessed is under the control of the address counters or the microprocessor. When the waveform is running, U10A pin 12 is high thus selecting the 'B' inputs to the data selectors. This connects the outputs of the waveform address counter to the address bus of the waveform memory. When the microprocessor is accessing the waveform memory, $\overline{\text{ARBMEM}}$ (U5B pin 12) goes low. AS (U2C pin 5) then clocks this low through the flip flop U5B, setting U5B pin 8 high. This forces U10A pin 12 low, selecting the 'A' inputs to the data selectors. This connects a portion of the microprocessor's address bus (ADR13-ADR1) to the waveform memory address bus. The microprocessor is then able to write to or read from any location in the waveform memory. $\overline{\text{ARBMEM}}$ originates in the address decoding section of the microprocessor. AS (address strobe) is a continuously running output of the microprocessor. The signal labeled $\overline{\text{SELOVR}}$ is an output of the microprocessor section. When a return to start is initiated by the user, the waveform is held at its current address. $\overline{\text{SELOVR}}$ holds the address select line (U10A pin 12) high and maintains the waveform memory at the location determined by the address counter. The microprocessor can then read the current data in the waveform memory in order to calculate a ramp back to the starting value.

4.2.1.4 Waveform Memory

Refer to schematic 0103-00-1389, sheet 3. The main components of the waveform memory are two random access memories (U11 and U12) and two octal bus transceivers (U16 and U17). The random access memories (RAM) each contain 8,192 memory locations with each location 8 bits wide. The location to be accessed is determined by the 13 bit binary number on the RAM address bus (A12-A0). If data is to be written into the RAM, pin 27 (Write Enable) is pulsed low. If data is to be read from the RAM, pin 22 (Output Enable) is pulsed low. The chip select (pin 20) must be low to enable any activity to the RAM. The bus transceivers act as two way gates between the waveform memory and the microprocessor's data bus. When U16 pin 19 (EN) is high, the transceiver enters a high impedance state and no data is transferred through it. When pin 19 (EN) is low, the direction of data transfer is determined by pin 1 (DIR). If pin 1 (DIR) is high, data is transferred from the 'A' side to the 'B' side. When pin 1 is low, the direction of transfer reverses.

The waveform memory is setup in a '2 port' configuration. From the microprocessor's point of view, the waveform memory appears as one RAM that is 16,384 locations deep by 8 bits wide. In this configuration, U12 contains all the even numbered locations and U11 contains all the odd numbered locations. To the waveform synthesizer the waveform memory appears as one RAM that is 8,192 locations deep by 16 bits wide. The four least significant bits are used for control and the upper 12 (WBIT12-WBIT1) are the waveform data bits.

The microprocessor accesses the waveform memory for several reasons; to fill it with waveform data, to read or change waveform data at a specific location or to set the control bits. To write to or read from one 16 bit wide waveform memory location,the microprocessor must execute two 8 bit write or read cycles. When the microprocessor accesses the waveform memory, $\overline{\text{ARBMEM}}$ (U5B pin 12) goes low. AS (U2C pin 5) clocks this low through the flip flop U5B which sets pin 9 low. Thus, the state of the chip selects for the waveform memory RAMs (U15A pin 1 and U15B pin 4) depend upon ADR0 (U8A pin 1), which is the least significant bit of the microprocessor address bus. When an even numbered memory location is addressed, ADR0 is low setting $\overline{\text{CS0}}$ (U15A pin 1) low and enabling U12. Since $\overline{\text{CS1}}$ (U15B pin 4) is high at this time, U17 is also enabled. If this is a write cycle $\overline{\text{R}}$/W (U5A pin 2 and U17 pin 1) is high. Data (AD7-AD0) (U30) then flows through U17 from the microprocessor to U12. This also sets $\overline{\text{AWE}}$ (U4A pin 3) low which causes U12 to accept data. If an odd numbered memory location is being addressed, the same sequence occurs except U8A Pin 1 (ADR0) is high selecting U11 and U16. During a read cycle, $\overline{\text{R}}$/W is low. This changes the direction of transfer through U16 and U17 and sets $\overline{\text{AOE}}$ (U6A pin 3) low which forces the selected RAM to output data. The two lines, E (U3D pin 12) and EB (U4A pin 2) are continuously running signals that originate in the microprocessor section. They are used to synchronize data transfer during read and write cycles. Waveform memory read and write timing is shown in Figure 4-2A and B.

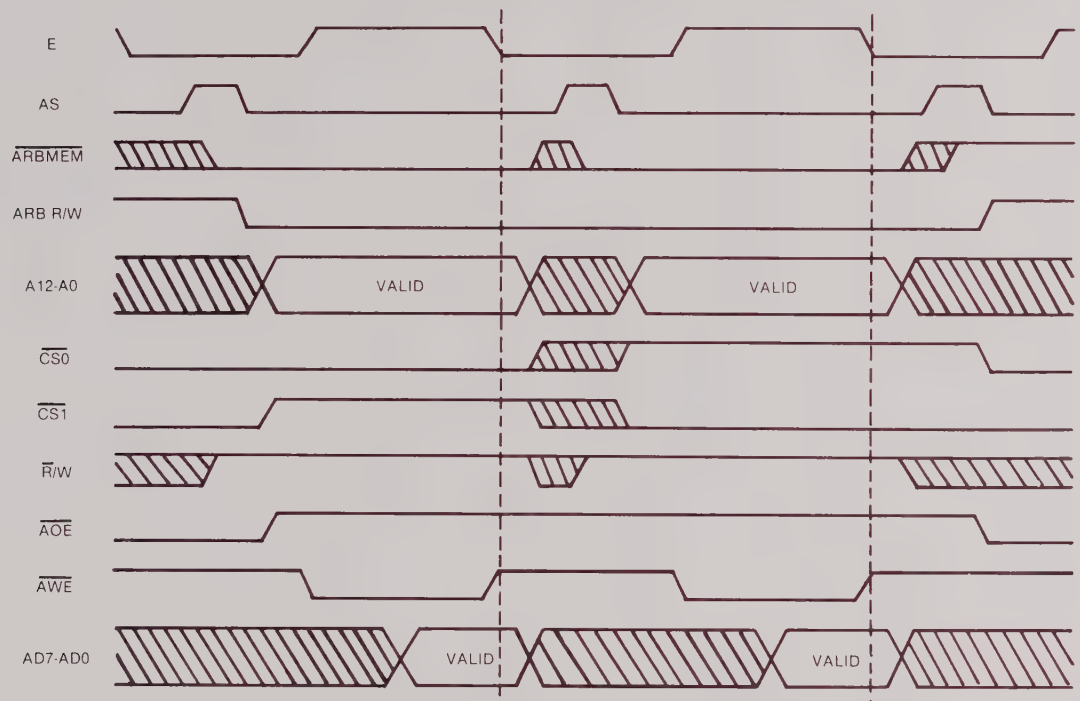


Figure 4-2A. Two Consecutive Write Cycles to Waveform Memory

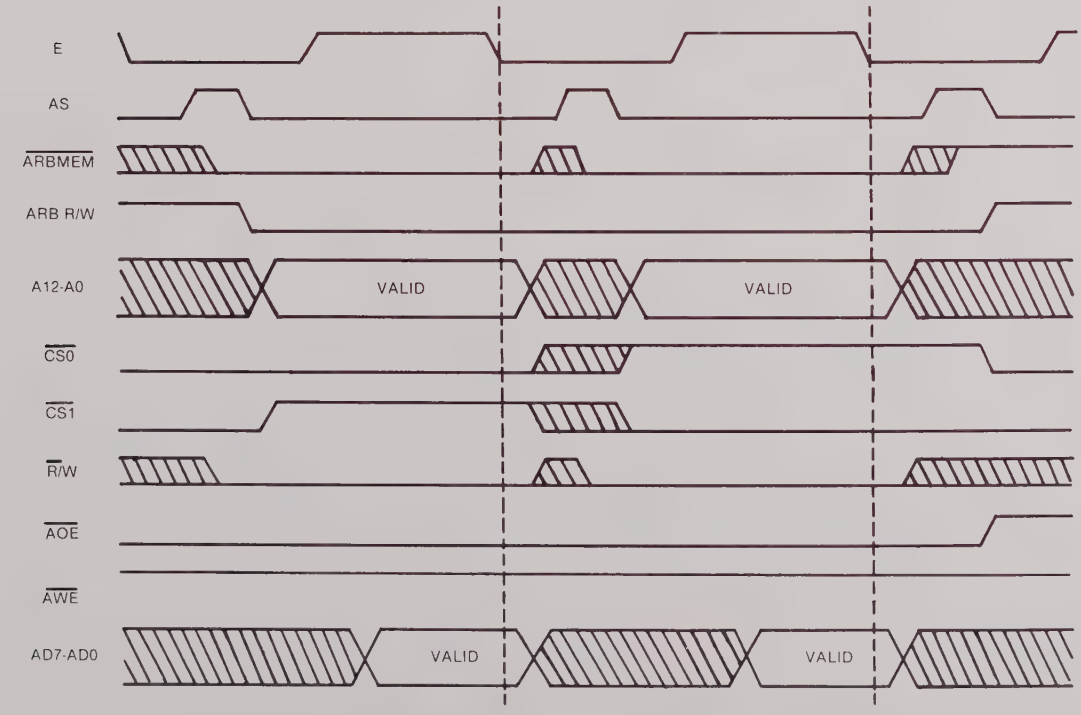


Figure 4-2B. Two Consecutive Read Cycles From Waveform Memory

NOT VALID

Both RAMs in the waveform memory (U11 and U12) obtain their power from the battery backed up power supply (BBV). BBV is maintained at 2V or greater even when the instrument is turned off. This allows the waveform memory to retain it's waveform data. When the instrument power is off, the output enable (pin 22) for the RAMs is low. Since the RAMs still have power, they must be disabled or they will try and drive their data bus, consuming more power and draining the battery. The analog switch, U7A and U7B, and it's control line ($\overline{MR}$) facilitate this by floating the chip select lines to the RAMs when the instrument power is turned off. This allows the resistors, R25 and R26, to pull the chip selects (U11 and U12 pin 20) high thus disabling the RAMs. The switches are controlled by $\overline{MR}$ (U7A pin 5) from the power on/off reset circuit (ref:schematic 0103-00-1389 sheet 2). When the instrument power is turned off $\overline{MR}$ goes low which opens the switches and the RAMs are disabled. As the instrument power is turned on, $\overline{MR}$ (U7A pin 5) is held low. After the microprocessor has stabilized, $\overline{MR}$ returns high which then closes the switches in U7 and allows for normal operation.

As mentioned before, the waveform memory is 8,192 locations deep and 16 bits wide. Of these 16 bits, the four least significant in each location are control bits. These bits are ZBIT (U11 pin 11), SBIT (U11 pin 12), STBIT (U11 pin 13) and $\overline{LOAD}$ (U11 pin 15). The function of $\overline{LOAD}$ is to restart the waveform at the start address. $\overline{LOAD}$ is set to a low in the memory location defined by the user as the waveform stop address. When this location is accessed $\overline{LOAD}$ causes the waveform address counter to restart. STBIT is used to stop the waveform in the 'triggered' modes. STBIT is set to a low at locations defined by the user as breakpoints. It is clocked through the waveform latch and sent to the Trigger and Hold logic section. If the instrument is set to a 'triggered' mode, a low STBIT will cause the trigger logic to stop the waveform. The Sync Out connector is driven by the control bit SBIT. This bit is set to a low at the location defined by the user as the sync address. SBIT is clocked through the waveform latch then buffered by U12A and output to the Sync Out connector (ref: schematic 0103-00-1456 sheet 3). ZBIT controls the Z-Axis output. This bit is set by the microprocessor at locations in waveform memory where cursors and thumbtacks occur. Its logic polarity is set by the user. If negative Z logic is selected, ZBIT is set to a high. If positive Z logic is selected, ZBIT polarity is reversed. ZBIT is clocked through the waveform latch and sent to the Z-Axis driver circuit (ref:schematic 0103-00-1456 sheet 3).

The upper 12 bits of each memory location contain the waveform data. Of these 12 bits (WBIT1-WBIT12), WBIT1 is the most significant and WBIT12 is the least significant. The microprocessor calculates the waveform data based on user input and places that data into the user defined memory locations. The data is then sequentially accessed to be output to the waveform synthesizer.

4.2.1.5 Waveform Latch

Refer to schematic 0103-00-1456, sheet 3. The main components of the waveform latch are two octal D type flip flops. The information present on the D inputs (pins 3,4,7,8,13,14,17 and 18) is transferred to the Q outputs (pins 2,5,6,9,12,15,16 and 19) on the rising edge of the clock (pin 11). The data on the Q outputs is held until the next clock. The purpose for the latch is twofold. The first is to ensure that the waveform data is valid before being applied to the waveform synthesizer. When a location of waveform memory is accessed, the data bits take a certain amount of time to reach their final state. When the next clock pulse occurs, the data has become valid and is clocked through to the waveform synthesizer. The clock for this circuit is the same clock used in the waveform address counter. Because of this, the address for the next waveform memory location is being applied to the waveform memory while the current data is being latched through to the waveform synthesizer.

The second function of the waveform latch is to allow the microprocessor to access the waveform memory without erroneous data being applied to the waveform synthesizer. When the microprocessor accesses the waveform memory, ARB R/W (U24A pin 1) goes low. This clears the flip flop, U24A, and forces pin 5 low which turns off the clock to the latches. Because the waveform clock and the microprocessor are running asynchronously it is possible for pin 5 of U24A to go low in the middle of a clock pulse. This could result in improper operation of the latches; i.e. no data latched through or erroneous data latched through. To prevent this U17A, U17B, U17C, U27D, U20B and U22B are configured as a 'whole pulse circuit'. This circuit assures that if a clock pulse (U27D pin 13) has started when the clock turn off signal (U24A pin 5) occurs, the whole pulse will reach the latches before the clock is shut off. Once the memory access is finished, ARB R/W (U24A pin 1) goes high. $\overline{EB}$ then clocks this high through the flip flop to pin 5 which turns the clock to the latches back on. Once again the 'whole pulse circuit' assures that only the next complete clock pulse will reach the latches. NO LOAD (U24A pin 6) is high when the microprocessor is accessing the waveform memory. It's function is discussed in paragraph 4.2.1.2.

The 'nand' gate U20A is used during a return to start. During normal operation neither GATE (U20A pin 2) nor BURST (U20A pin 1) are asserted high at the same time. When a RETURN is initiated by the user, the microprocessor sets both of these signals high. This pulls

SYNCEN (U20A pin 3) low which turns off the clock to the latches. SYNCEN is also used in the Trigger and Hold logic to disable any external sync in pulses that may occur during this time. As previously described, the address counter is always one address past the current waveform address. With the latches holding the current waveform data, the microprocessor is free to manually clock the waveform address counter from its present address to the address of the current waveform data. Once the current address is reached and its data read, the microprocessor releases SYNCEN and manually clocks the waveform memory and the latches through the return to start ramp.

4.2.1.6 Waveform Synthesizer

Refer to schematic 0103-00-1456, sheet 4. The function of the waveform synthesizer is to convert the digital data from the waveform memory to an analog voltage. The main components of the waveform synthesizer are a 12 bit digital to analog converter (U2) and two operational amplifiers (U6 and U7). A simplified diagram of the waveform DAC is shown in figure 4-3. The DAC (digital to analog converter) sinks a current into the DAC OUT (pin 9). That current is proportional to the binary number appearing on it's digital inputs (WF1-WF12) and the current applied to the reference input (pin 6). WF1 is the most significant bit (MSB) and WF12 is the least significant bit (LSB) of the binary waveform data. The reference current is determined by the precision 10V reference at the reference out (pin 4) applied to an internal reference resistor connected to pin 6. The reference voltage is also applied to the internal bipolar offset resistor connected to pin 8. This adds a constant current to the DAC OUT equivalent to the half scale output current, thus causing the net output current to be bipolar. Resistors R31 and R32 are connected in series with the internal reference and offset resistors. Their values are staggered to force the zero output current condition to occur at a binary code of 100000000000. The binary codes applied to the DAC range from 000000000001 to 111111111111. The op amp, U6 converts the output current of the DAC to a voltage. The internal resistors connected to U2 pins 10 and 11 are used for feedback from U6. These resistors are matched to the other resistors internal to the DAC, thus ensuring good gain accuracy and temperature tracking. The inverting input (pin 2) of the op amp acts as a current summing node and is kept at virtual ground. The output current of the DAC flows into the summing node and through the 2.5kΩ feedback resistance to create a voltage at U6 pin 6 whose full scale value is ±2.5V.

The op amp U7 and the resistors in RN1 act as an inverting summing amplifier for the internal and external waveforms. For internal waveforms U7 provides a

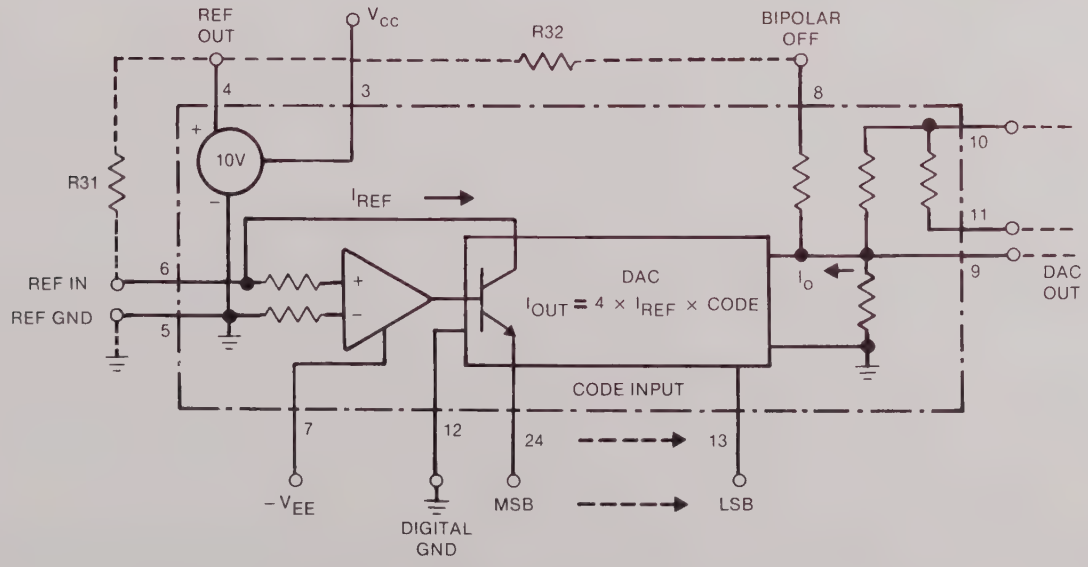


Figure 4-3. Waveform DAC Functional Diagram

gain of −0.8, changing the full scale waveform to ±2V. For external waveforms applied to the Sum In input, U7 provides a gain of −0.4, converting a ±5V waveform to ±2V. At the Sum In input, R34 provides a precision 50 ohm termination for the external waveform. The fuse, F1, and the zener diodes, CR14 and CR15, protect against excessive voltage. The resistance of the fuse causes some gain error from the Sum In input and can be replaced with a jumper if greater accuracy is required.

4.2.1.7 Amplitude Control

Refer to schematic 0103-00-1456, sheet 4. The amplitude control circuit consists of a multiplying DAC (U9) and an op amp (U8). The DAC has 12 bits of resolution but only 10 are used, so the 2 least significant (pins 14 and 15) are tied low. A simplified diagram of the DAC is shown in figure 4-4. The DAC produces a voltage at VOUT (pin 17) that is proportional to the binary number applied to it's digital inputs (AMP1-AMP10) and the voltage applied to VREF (pin 1). The waveform is applied to the VREF input and is attenuated by the ratio of D/1024; where D is the decimal equivalent of the binary number at the digital inputs to the DAC. The waveform attenuation at this point is typically over a 10:1 range; 1000/1024 to 100/1024 while the output attenuator provides 3 separate decades of attenuation. The value of the peak amplitude and offset as set by the user determine the attenuator range selected by the microprocessor. The microprocessor then programs the amplitude control to the appropriate attenuation within the range. If the value of the offset requires the output attenuator to be in the range of least attenuation and the amplitude is set below this range, the amplitude control can cover a range of up to 1000:1. Because the waveform is bipolar, the power supplies to the DAC are also bipolar. The positive supply is +10V with the digital ground tied to −5V. This biases the internal switches of the DAC at such a point that the negative voltage swings of the waveform will not affect them. The levels of the digital inputs are −5V for a logical low and +5V for a logical high to properly control the internal switches. This amplitude information originates in the microprocessor and is interfaced to the amplitude control by the control shift register (ref:schematic 0103-00-1456 sheet 2). The op amp, U8 acts as a buffer for the DAC and has a gain of one.

4.2.1.8 Offset Control

Refer to schematic 0103-00-1456, sheet 4). The components of the offset control circuit are a 12 bit multiplying DAC (U5) and an op amp (U4). A simplified diagram of the DAC is shown in figure 4-4. The DAC (U5) is the same type used in the amplitude control circuit, but it is configured here in the current output mode. This is done by connecting a reference to the voltage output

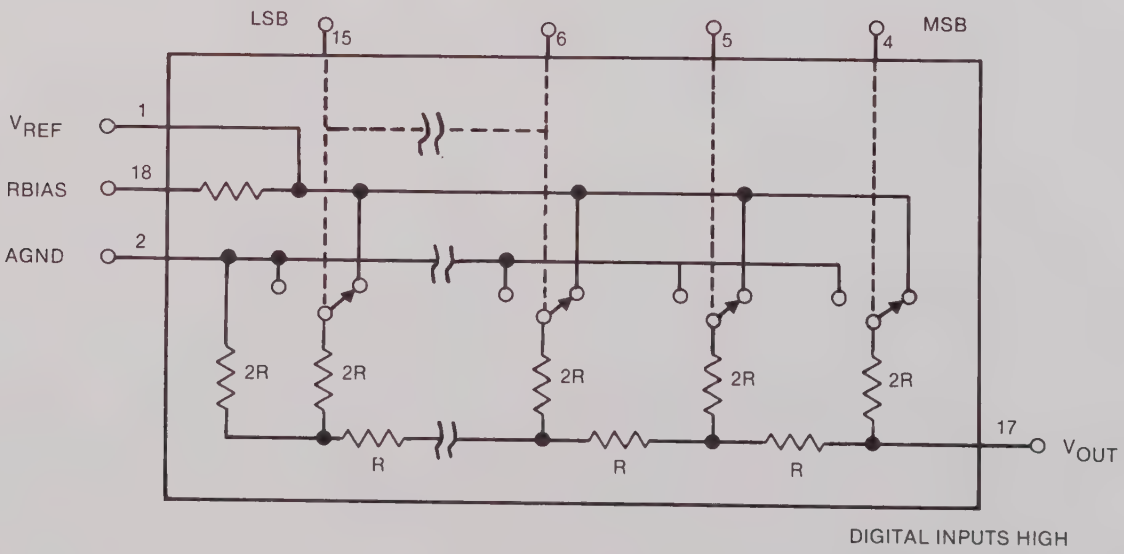


Figure 4-4. Multiplying DAC Functional Diagram

(pin 17) and taking the current output from VREF (pin 1). The current output is proportional to the binary number applied to the digital inputs (OFF1-OFF12) and the voltage applied to pin 17. That reference voltage is taken from the precision reference in the waveform DAC. The resistor on pins 1 and 2 of RN2 provides extra current drive capabilities for the 10V reference. As with the amplitude data, the offset data (OFF1-OFF12) originates at the microprocessor and is interfaced to this circuit by the control shift register (ref:schematic 0103-00-1456 sheet 2). Because of this the logic levels of the offset data are ±5V and the DAC requires the +10V and −5V power supplies. The op amp (U4) converts the current output of the DAC to a voltage. The feedback resistor for the op amp is internal to the DAC to ensure better accuracy. The inverting input of the op amp (pin 2) acts as a summing node and is held at virtual ground. The output current of the DAC flows into the summing node and through the feedback resistor to create a voltage whose nominal swing is −2.5V to −7.5V as the offset is changed from −5V to +5V. The same attenuator ranging that applies to the amplitude control circuit also applies to the offset. When the Calibration constant is set during calibration, the microprocessor adds a digital offset constant to the offset data (ref:Section 5, Calibration). This constant allows the offset circuit to compensate for the offset errors throughout the analog signal path and eliminates the need for an internal calibration adjustment.

4.2.1.9 Output Amplifier

Refer to schematic 0103-00-1456, sheet 4. The output amplifier provides the final waveform amplification and output drive for the instrument. It consists of a discrete inverting amplifier for the high frequency component of the waveform with an op amp to provide DC stability and a low frequency signal path. A simplified model of the amplifier is shown in figure 4-5. Pin 5 of RN2 acts as a current summing node for the amplifier. The waveform is summed into the amplifier through pin 4 of RN2 with a gain of 5.12. The offset control voltage is summed into the amplifier through pin 3 of RN2 with a gain of 4.096. The 10V reference is also summed into the amplifier through pin 2 of RN2. This creates an current equivalent to the mid scale current from the offset voltage, thus making the offset control bipolar.

High frequency signals drive the symmetrical common emitter stage of Q7 and Q8 through C44 and C45. DC and low frequency signals drive this stage through the

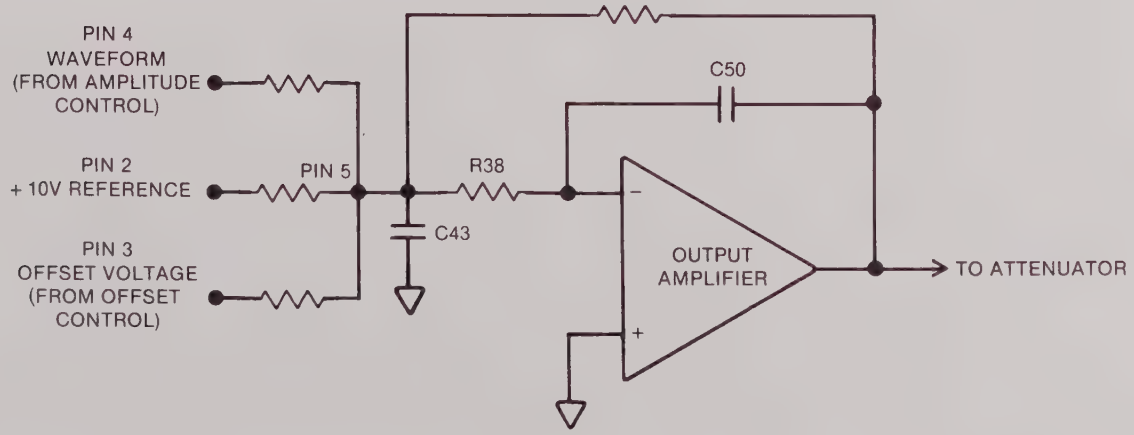


Figure 4-5. Output Amplifier Simplified Diagram

op amp U10. The output of U10 modulates the bias voltage at the bases of Q7 and Q8. This common emitter stage provides the voltage gain for the amplifier and drives the emitter followers, Q9 and Q10. These transistors provide the current gain and drive capabilities for the amplifier. The resistor, R45, and diodes, CR16 and CR17, serve to keep the output transistors biased on, thus removing crossover distortion. The output waveform, which is 20V p-p maximum, is fed back to the summing node through the resistors on pins 7 and 6 of RN2. The capacitors, C50 and C43, and the resistor, R38, create an active low pass filter with the amplifier. This helps to improve the signal to noise ratio of the output waveform. The RC networks of R48,C51 and R49,C52 improve the frequency response of the amplifier.

4.2.1.10 Attenuator

Refer to schematic 0103-00-1456, sheet 4. The output attenuator contains 3 strings of a resistor divider network, 2 SPDT relays to switch them in and out and 2 transistors to control the relays. The equivalent resistances of the divider strings are as follows; 5k ohms (R54), 555 ohms (R55,R56) and 55.5 ohms (R57,R58,R59,R60). The lines that control the relays (A0,A1) originate from the microprocessor and interface to this circuit from the control shift register (ref:schematic 0103-00-1456 sheet 2). The logic levels of these signals are ± 5V. The relays are shown in the energized position on the schematic. The function of this circuit is to attenuate the output waveform in three single decade steps. The configuration for these steps is shown in figure 4-6. The fuse, F1, protects the internal circuitry from excessive current applied to the output connector. The zener diodes, CR20 and CR21, protect against excessive voltages.

4.2.1.11 Shifted Logic Power Supply

Refer to Schematic 0103-00-1456, sheet 4. The shifted logic power supply contains a − 5V regulator (VR1) and a + 15V regulator (VR2). This circuit supplies the + 10V and − 5V for the control shift register, the amplitude control and the offset control. VR1 postregulates the − 15V supply down to − 5V with C38 acting as a filter capacitor. The + 15V power supply is connected to the input of VR2 and its common pin is tied to − 5V. The output of VR2 is regulated 15V above its common and is therefore + 10V. C39 acts as a filter capacitor for the + 10V supply.

4.2.1.12 Z-Axis Driver

Refer to schematic 0103-00-1456, sheet 3. The Z-Axis driver provides the output drive and level control for the Z-Axis output. The transistor Q6 acts as a programmable constant current sink. With Q1 off, the voltage developed across R25 sets the upper level of the Z-axis output.

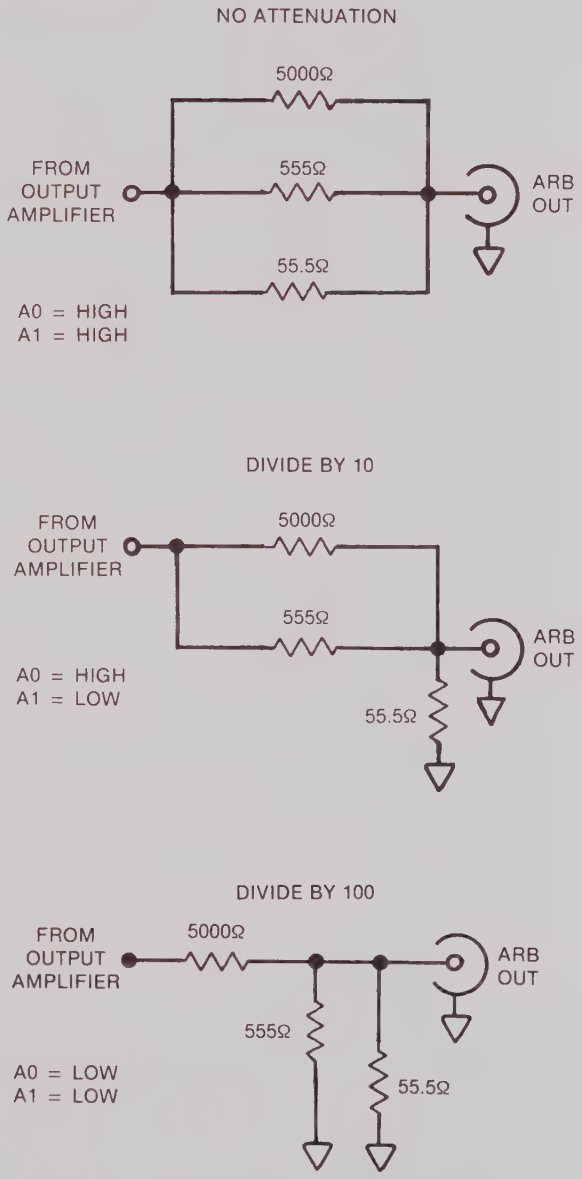


Figure 4-6. Attenuator Range Switching

The transistors Q2, Q3,and Q4 are current sources that can be individually enabled to supply current to the emitter resistors of Q6. As more current is supplied, less is required through R25, thus changing the voltage across R25 and the Z-axis level. The base of Q1 is driven by the ZBIT which originates in the waveform memory. The collector of Q1 in turn drives the emitter follower, Q5.

When ZBIT is high Q1 is turned on, pulling its collector voltage low. This turns off Q5 so the output is pulled low through R28. When ZBIT is high Q1 is turned off so the collector voltage is set by Q6. The output tracks this voltage minus the Vbe drop of Q5. R29 and R30 provide the 600 ohm output impedance of the circuit. Q2,Q3 and Q4 are controlled by the lines ZL0,ZL1 and ZL2. The lines originate in the microprocessor and are interfaced to this circuit by the control shift register (ref:schematic 0103-00-1456 sheet 2).

4.2.2 Timing And Triggering

4.2.2.1 General Description

The waveform clock controls the waveform address counter and thus the sample frequency of the waveform. The frequency of the waveform clock is generated either in the frequency synthesizer, set by the user as sample frequency or by an external reference. The trigger and hold logic contains the circuitry to select which reference is used and control the clock in the triggerable modes. The burst counter works in conjunction with the trigger and hold logic to control burst mode and acts as the internal waveform counter.

4.2.2.2 Frequency Synthesizer

Refer to schematic 0103-00-1456, sheet 2. The frequency synthesizer consists of two main circuit blocks, the phase lock loop (PLL) and the frequency range dividers. The main components of the PLL are a crystal reference (Y1), phase detector/divide by "N" (U36), dual op amp (U30), a voltage controlled oscillator (U31), a dual JK flip flop (U32) and a eight input data selector (U37).

In general terms, the phase detector (U36) compares the VCO (U31) frequency with the crystal reference frequency and sends a correction voltage to the VCO. This maintains the VCO frequency at the same accuracy as the crystal frequency. Before this comparison takes place, the crystal is divided by 6,144 to 1Khz. The VCO frequency is also divided down to 1Khz by a number "N" which is programmable. Changing "N" causes the VCO frequency to change to maintain the 1Khz to the phase detector and therefore the output frequency of the PLL changes. Both the divide by 6,144 and the divide by "N" are internal to U36. The divide by "N" is programmed by the microprocessor through the lines SERC, SERD and PLLE (U36 pins 10, 11 and 12). The microprocessor serially shifts in 16 bits of data on SERD, using SERC to clock it in. When all 16 bits have been shifted in, PLLE is pulled high to enable the new data. Of the 16 bits, 14 program the divide by "N" and 2 are present on U36 pins 13 and 14 (SW1 and SW2). These 2 bits control the data selector U37 which selects either the VCO frequency, VCO/2 frequency or VCO/4 frequency to be applied to the divide by "N" on U36 pin 9.

The phase detector in U36 compares the phase of the 1Khz reference to the phase of the 1Khz from the VCO and outputs correction pulses on pin 6 (PD). This pulse can be either positive or negative depending upon the direction of the phase difference. U30A, R8 and C8 act as an integrator to convert the pulses to a DC control voltage. U30B, R9 and C9 provide a low pass filter to stabilize the loop. The control voltage is then applied to the frequency control input of the VCO (U31 pin 13). The combination of the voltage on pin 2 and the capacitor C11 determine the frequency range of the VCO. U32A and U32B are flip flops configured as divide by 2's. These provide the VCO/2 frequency and the VCO/4 frequency. U37 selects one of the 3 different frequencies applied to the D0-D3 inputs based on the two bit binary number on it's A and B control inputs (pins 11 and 10). The selected frequency appears on the output at pin 6. The PLL divider switching and VCO frequency is shown in table 4-1.

The frequency range divider consists of four dual bi-quinary counters (U28, U33, U34 and U35) and one 8 bit data selector (U29). The counters (U35, U34, U33 and U28A) are configured as seven discrete divide by 10's. The output of the PLL is applied to the string of dividers to produce eight different decades of frequency range. The microprocessor controls the data selector (U29) with three lines; FRBIT1 (U29 pin 9), FRBIT2 (U29 pin 10) and FRBIT3 (U29 pin 11). The data selector uses the binary number from these three lines to determine which frequency range appears at its output on pin 5. U28B divides this frequency by 5 and the final frequency synthesizer output appears on pin 9 (INTREF). A truth table for the frequency range control is shown in table 4-2.

Table 4-1. PLL Switching and VCO Frequency

Display Counts	SW1 U36-13	SW2 U36-14	VCO Frequency U31-8
19998 – 16000	1	1	9.999 MHz – 8.000 MHz
15998 – 8000	1	0	7.999 MHz – 4.000 MHz
7998 – 4000	0	1	7.998 MHz – 4.000 MHz
3998 – 2000	0	0	7.996 MHz – 4.000 MHz
2.000 MHz	1	1	10.000 MHz

Table 4-2. Frequency Ranging

Sample Frequency Range	FRBIT1 U29-9	FRBIT2 U29-10	FRBIT3 U29-11
2 MHz – 200 kHz	1	1	1
199.98 kHz – 20 kHz	1	1	0
19.998 kHz – 2 kHz	1	0	1
1.9998 kHz – 200 Hz	1	0	0
199.98 Hz – 20 Hz	0	1	1
19.998 Hz – 2 Hz	0	1	0
1.9998 Hz – 200 mHz	0	0	1
199.98 mHz – 20 mHz	0	0	0

4.2.2.3 Trigger and Hold Logic

Refer to schematic 0103-00-1456, sheet 3. The trigger and hold logic can be broken up into circuit blocks. These are; reference selector, whole pulse circuit, trigger and mode control, and miscellaneous I/O.

The reference selector is made up of three "inverters" (U12D, U25E and U25D) and three 2 input "nand" gates (U16C, U26C and U21C). The internal reference from the frequency synthesizer is applied to this circuit on pin 9 of U25D (INTREF). Any external reference frequency applied to the Ref In connector appears at U12D pin 9 (REF IN). As with all digital inputs Ref In is protected against overvoltage by diodes, in this case CR3 and CR4. The microprocessor determines which signal is used with the line REFSEL (U25E pin 11). This line is interfaced to this circuit from the control shift register (ref: schematic 0103-00-1456 sheet 2). When REFSEL is high the internal reference frequency is gated through U26C and appears on U21C pin 8. To select the external reference frequency, the microprocessor sets REFSEL low.

The whole pulse circuit turns the waveform clock on and off. It consists of three 2 input "nand" gates (U16A, U16D and U16B), one 3 input "nand" gate (U22A) and two "exclusive or" gates (U15A and U15D). The reference frequency is applied to this circuit on pin 1 of U15A. U16A pin 1 is considered the "run" control. When the "run" is high the reference frequency passes through the circuit to U15D pin 11 (CLK). When "run" is low the reference frequency is blocked and CLK is off. Because the "run" control and the reference frequency are running asynchronously, "run" can change states in the middle of a clock pulse. The resulting narrow pulse would adversely effect the circuitry driven by the waveform clock (CLK). The whole pulse circuit prevents this by allowing the clock to finish its current pulse before it is shut off. The resistor on pin 12 of U22A and all the resistors in RN3 serve as pull up resistors to interface logic levels between different logic families. PCLK (U15D pin 13) is used by the microprocessor to manually drive the waveform clock. During a RETURN, the microprocessor asserts MANHOLD (U27B pin 4) to stop the waveform clock and then pulses PCLK to clock the waveform memory through the return ramp.

The trigger and mode control consists of three D flip flops (U24B, U23A and U23B) and the logic gates surrounding them. This circuit is controlled by the mode information from the microprocessor and the trigger inputs, both manual and external. The mode control bits originating at the microprocessor are; $\overline{\text{CONT}}$, GATE, TGL, and BURST. These control lines are interfaced to this circuit from the control shift register (ref: schematic 0103-00-1456 sheet 2). The truth table for the mode control bits is shown in table 4-3.

Table 4-3. Mode Control

Mode	CONT U23-10	GATE U21-4	TGL U15-9	BURST U21-12
Continuous	Low	Low	Low	Low
Triggered	High	Low	Low	Low
Gated	High	High	Low	Low
Toggled	High	High	High	Low
Burst	High	Low	Low	High

The function of the trigger section is to control the "run" signal to the whole pulse circuit which in turn controls the waveform clock (CLK). In continuous mode, $\overline{\text{CONT}}$ (U23B pin 10) is held low. This sets the flip flop U23B which pulls the Q (pin 8) of U23B low and turns on the waveform clock (CLK). When triggered mode is selected, $\overline{\text{CONT}}$ is set high. The next waveform clock pulse clocks the high through U23A which clears U23B and sets its $\overline{\text{Q}}$ (pin 8) high. With that line high, the break points in the waveform memory are used to stop the waveform clock by driving U26B pin 4. The flip flops of U23 are immediately reset to wait for a trigger pulse on the clock input (pin 11) of U23B. When a break point is encountered in the waveform memory, $\overline{\text{STOP}}$ (U1 pin 15, ref: schematic 0103-00-1456 sheet 3; waveform latch) is pulled low. $\overline{\text{STOP}}$ is gated with NO LOAD at U15D (ref:schematic 0103-00-1389 sheet 3) to set TPOINT high. NO LOAD inhibits accidental break points when the microprocessor is accessing the waveform memory. TPOINT (U22C pin 11) forces U26B pin 4 high which turns off the waveform clock (CLK).

When a trigger pulse is applied to the Trig In connector, it is gated through U12B, U15B, U15C, U26D, and U26A so that a positive pulse appears at the clock input of U23B. Since the D input (pin 12) is high, the $\overline{\text{Q}}$ output (pin 8) is pulled low which turns on the waveform clock until

the next break point is encountered. The flip flops of U23 are reset after each trigger. When the manual trigger key is pressed, the microprocessor toggles SLOPE (U15B pin 5). That creates the same sequence of events as an external trigger. SLOPE (U15B pin 5) is also used to control the trigger slope of the external trigger signal. When positive trigger slope is selected, SLOPE is set high. When negative trigger slope is selected, SLOPE is set low. While the trigger slope is being changed, the microprocessor sets $\overline{\text{TRIGMASK}}$ (U23B pin 12) low to prevent the change in state of SLOPE from causing a trigger.

The operation of gated mode is similar to triggered except an additional requirement must be met before a break point will stop the waveform clock. The GATE bit (U21B pin 4) is set high by the microprocessor. As long as the trigger input is asserted, U21B pin 5 is held high and TPOINT is not gated through U22C. Once the trigger input is released, U21B pin 5 goes low and allows the next TPOINT through U22C to stop the waveform clock.

When toggle mode is selected, the microprocessor sets TGL (U15C pin 9) and GATE (U21B pin 4) high. This disables the trigger path through U26D and enables the flip flop U24B, which is configured as a divide by 2. Every rising edge on the clock input of U24B (pin 11) causes U21B pin 5 to change states. This means toggled operation is the same as gated except the control line at U21B pin 5 is set high by a trigger pulse and held until the next trigger pulse.

Burst mode is similar to gated and toggled in that more than one condition must be met to stop the waveform clock and thereby the waveform. When burst mode is selected, the microprocessor sets BURST (U21D pin 12) high and sends the selected burst count to the burst counter (ref: schematic 0103-00-1389 sheet 4). When a trigger pulse clocks U23B, it's $\overline{\text{Q}}$ (pin 8) goes low to start the waveform clock. The Q output of U23B (pin 9) goes high and loads the burst count into the burst counters. The output of the burst counter is $\overline{\text{STOPOK}}$ (U21D pin 13). This line is held high until the selected burst count is reached. While it is high TPOINT is stopped at U22C. When the burst count is reached, $\overline{\text{STOPOK}}$ is pulled low and the next TPOINT is allowed through U22C to stop the waveform clock. The Burst Done Output (U25B pin 4) is simply an inverted version of the TPOINT signal and tells the outside world that the waveform is stopped.

The Hold In input works in much the same way as the trigger control circuitry in that it controls the "run" signal to the whole pulse circuit and thus the waveform clock. When a low is applied to the Hold In connector it appears at U21F pin 13 (HOLD IN). This pulls U27C pin 10 low and turns off the "run" signal. When the hold key is pressed, the microprocessor pulls $\overline{\text{MANHOLD}}$ (U27B pin 4) low which also turns off the "run" signal.

The Sync In and Return In inputs are also routed through the trigger and hold logic. A low applied to the Return In connector appears at U12E pin 11 (RETURN IN). The output of U12E (pin 10) is sent to the microprocessor section where it is treated the same as a key press. The Sync In input is connected directly to U21A pin 1. The output of U21A ($\overline{\text{SYNC IN}}$) is sent to the waveform address counter where it will restart the waveform when asserted. The signal SYNCEN originates in the waveform latch (ref: schematic 0103-00-1456 sheet 3). It's function is to block any sync input while the microprocessor is setting up a return to start. It is pulled low during this time.

4.2.2.4 Burst Counter

Refer to schematic 0103-00-1389, sheet 4. The burst counter contains five programmable 4 bit binary counters (U50, U51, U43, U41, and U40) and three octal D type flip flops (U47, U42, and U44). The counters are cascaded to form a 20 bit binary counter with U50 pin 14 the least significant bit and U40 pin 11 the most significant. The microprocessor converts the decimal burst count set by the user to a binary number and writes the 1's compliment of that number to the preload inputs of the counters (pins 3,4,5 and 6 of U50, U51, U43, U41 and U40). For instance; if the burst count is set to the largest possible setting, 1,048,575, the preload inputs to the counters are set to all zeros. When the instrument is triggered, $\overline{\text{BURLOAD}}$ (U50 pin 9) is pulled low by the trigger and hold logic and loads the binary burst count into the counters. The counters are clocked by the waveform clock (U50 pin 2) but only count when BCEN (U50 pin 7) is high. BCEN is generated at the waveform address counter from the bit in the waveform memory that sets the waveform stop address; $\overline{\text{LOAD}}$ (ref: schematic 0103-00-1389 sheet 3). Since BCEN is high for only one clock pulse, the burst counter, starting at the preset number, increments one for every waveform that is output. When the burst counter reaches it's full value (all ones) the carry out on U40 pin 15 (STOPOK) is sent to the trigger logic to stop the waveform clock. It is also gated with the load pulse (ref: schematic 0103-00-1389 sheet 3; U15C) to force BCEN low and prevent further counting. This is done to prevent burst counter overflow if the microprocessor is accessing the waveform memory when a break point occurs.

The octal flip flops (U47, U42 and U44) act as data latches between the burst counter and the microprocessor data bus. This allows the microprocessor to read the current value of the burst counter and facilitates the internal waveform counter. When the instrument is in gated or

toggled mode the burst counter is preset to zero. When the user accesses the waveform counter, the microprocessor reads the current count directly and converts it to decimal for output to the display or communication port. When burst mode is selected, the microprocessor must read the counters and calculate the current count before it can be displayed.

The data on the inputs (pins 3,4,7,8,13,14,17 and 18) is constantly transferred into the latches on the rising edge of the clock on pin 11. The outputs (pins 2,5,6,9,12,15,16 and 19) however are in a high impedance state unless the output enable on pin 1 is low. When the microprocessor reads the counter value it does so in three read cycles, accessing each latch one at a time by pulling its enable (BC1, BC2 or BC3) low. Because the counter data is continuously changing, the clock to the latches must be turned off when they are being read. Also, the clock and the enable lines happen asynchronously so that erroneous data could be transferred across the latches if the enable occurred in the middle of a clock pulse. To control the clock, U38A, U48D, U38C, U48A, U48B, U48C and U38B are configured as a whole pulse circuit. This circuit ensures that a whole pulse is completed before the clock is turned off. The waveform clock is applied to this circuit at U48A pin 2. U48D pin 11 is the "run" control for the circuit. When this is high the clock is turned on at U48C pin 8 and is turned off when "run" is low. The enable lines are applied to U38A and when any one is pulled low the "run" control goes low to turn off the clock to the latches.

4.2.3 Instrument Control

4.2.3.1 General Description

Instrument parameters and waveform information are entered by the user through the front panel, electrical connectors and the communication port if installed. This information is processed by the microprocessor and memory section which in turn controls the appropriate dedicated circuit. Instrument status is reflected back to the user by the microprocessor and memory section through the display. The microprocessor and memory section is divided further into circuit groups which work closely with the microprocessor to form essentially one functional block. These are; power on/off reset, address decoder, main memory, battery circuit, front panel interface, control shift register and output ports. A description of the front panel is included in the front panel interface.

4.2.3.2 Microprocessor

Refer to schematic 0103-00-1389, sheet 2. The basic operation of the microprocessor can be described as "fetch and execute". In a continuously running cycle it fetches instructions from read only memory and executes them. To perform these tasks the microprocessor must read from and write to the external circuitry. Each device, or location in a device, that the microprocessor interfaces to has a unique address. To access these locations the microprocessor outputs the address and either inputs or outputs the data being transferred. When data is input to the microprocessor it is referred to as a read cycle and is called a write cycle when data is output from the microprocessor. The components that make up the functional microprocessor are; an 8 bit CMOS microprocessor (U30), a 4 MHz crystal (Y1), an octal 3-state transparent latch (U14), an octal line driver (U37A and U37B) and two gates of a quad 2 input 'exclusive or' gate (U34A and U34D).

The microprocessor (U30) has an internal clock generator whose frequency is based on the external crystal (Y1). The crystal frequency of 4 MHz is internally divided to produce 1 MHz "E" clock on pin 40. The "E" clock is used as a system clock to synchronize all data transfers by the microprocessor. The microprocessor uses a 16 bit address bus and an 8 bit data bus. The lower 8 address bits are time multiplexed with the 8 bit data bus on pins 37-30. The upper 8 bits of the 16 bit address bus appear on pins 22-29 (A15-A8) of U30. During the first portion of a read or write cycle, when the "E" clock is low, the lower 8 bits of the address bus appear on pins 30-37 (AD7-AD0) and during the last portion of the cycle, when the "E" clock is high, AD7-AD0 are used for the 8 bit data bus. Pin 39 of the microprocessor is the address strobe (AS). This is a 1 MHz clock whose falling edge is coincident with the valid address bus on AD7-AD0. The address latch (U14) is used together with AS to demultiplex the address and data buses. When a write or read cycle begins, the full 16 bit address appears on pins 22-37 of the microprocessor. AS (pin 39) goes high during this time and the lower 8 bits of the address are transferred to the outputs of U14 (pins 2,5,6,9,12,15,16 and 19). The address strobe (AS) then goes low and the lower 8 bits of the address bus are latched into U14. AD7-AD0 are used for data bus transfer for the rest of the cycle.

The line on pin 38 of the microprocessor is the read/write control (R/$\overline{W}$) where a high indicates a read and a low indicates a write. It is used by the external devices to determine if the microprocessor is executing a read cycle or a write cycle. The "E" clock, AS and R/$\overline{W}$ are gated together to create the various enable signals and synchronize bus timing for the external devices interfacing with the microprocessor. A diagram of the bus timing for the microprocessor is shown in figure 4-7. An inverted version of the read/write control called R/$\overline{W}$ is created by the "inverter" U2D and is used in the main

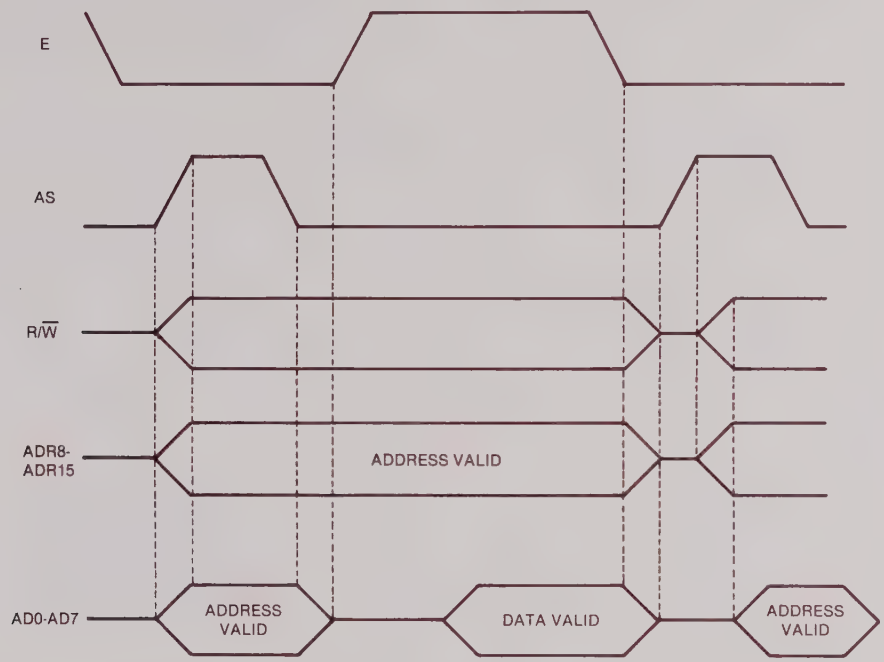


Figure 4-7. Multiplexed Microprocessor Bus Timing

memory and waveform memory sections to generate control lines. The 2 input "and" gate, U6D, is used to produce a buffered version of the "E" clock due to the limited drive capabilities of the microprocessor. The line drivers in U37 and the "exclusive or" gates in U34 are used as buffers and are transparent to the microprocessor and external circuitry. They provide improved drive characteristics for some of the microprocessor outputs.

Besides the address and data buses the microprocessor also has eleven pins configured as data outputs and one pin configured as a data input. U30 pin 13 (SERD) outputs the data, in a serial form, that controls the phase lock loop in the frequency synthesizer and the control shift register (ref: schematic 0103-00-1456 sheet 2). U30 pin 14 (SERC) is used as a clock to input the serial data into the shift registers in both circuits. U30 pin 15 (PLLE) and pin 16 (ANLE) are used to enable the new data to the phase lock loop and the control shift register respectively. U30 pins 17, 18 and 19 (FRBIT3, FRBIT2 and FRBIT1) control the frequency range dividers in the frequency synthesizer (ref:schematic 0103-00-1456 sheet 2). U30 pin 8 (KW1), pin 10 (KW2) and pin 20 (KM) are used by the microprocessor to interface to the knob interrupt circuit in the front panel interface (ref: schematic 0103-00-1389 sheet 3). This circuit provides the microprocessor with information from the control knob on the front panel. Pin 11 of U30 ($\overline{\text{BLOAD}}$) is used to place a temporary load on the battery to test its condition. Pin 12 of U30 (BTST) is configured as an input and is used to read the status of the battery during this test.

The interrupt input of the microprocessor is on pin 5 (IRQ). This input is held high by the resistor R15 unless it is pulled low by a circuit requesting service. When IRQ is pulled low the microprocessor stops its main program flow and begins a execution of an interrupt service routine. This routine begins by querying the various circuits as to what pulled the interrupt. Action is then taken to handle the needs of the interrupt. Once those needs have been met, main program flow resumes.

The RESET input of the microprocessor (U30 pin 6) is used to inhibit operation while the instrument power is being turned on or off. This prevents the microprocessor from outputting bad data and control bits that would disturb the instrument setup. When the instrument is first turned on, pin 6 is held low by the power on/off reset circuit until the power supplies and internal clock generator of the microprocessor have stabilized. When RESET does go high, the microprocessor automatically fetches data from the last two locations in memory. This data is the address of the memory location the microprocessor must access in order to begin normal execution.

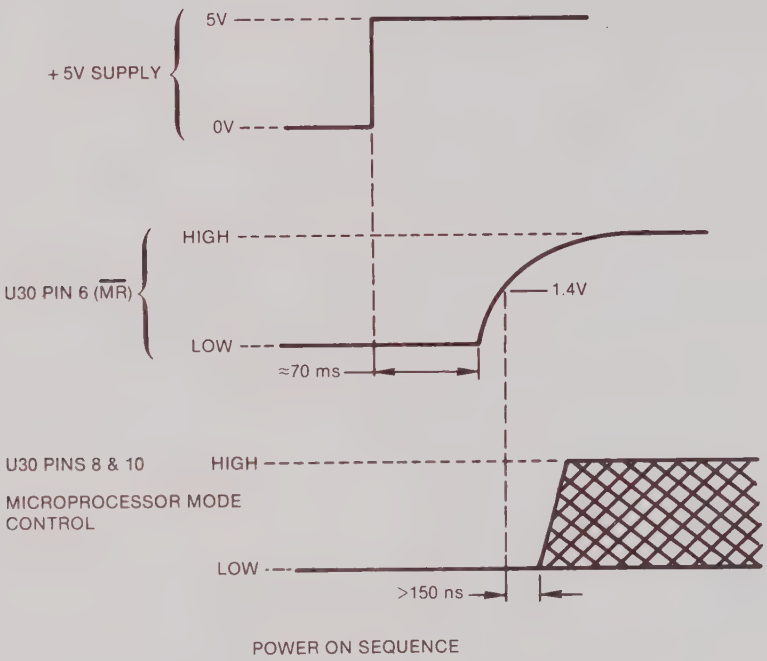


Figure 4-8. Power On/Off Reset

During normal operation the RESET line (pin 6) is held high by the resistor R4. When the power is turned off, U30 pin 6 is again pulled low before the falling power supplies disrupt microprocessor operation. The reset timing is shown in figure 4-8.

When the instrument power is turned off, the power on/off reset circuit pulls the STBY input of the microprocessor low (U30 pin 7). This forces the microprocessor into a low power standby mode before the battery becomes its sole power source. In this way battery life is extended. The timing for the STBY control is shown in figure 4-8.

The microprocessor used has several operational modes. The Model 75 uses what is called mode 2. This mode uses the multiplexed address and data bus as described earlier. The mode used is determined by the status of pins 8, 9 and 10 of U30 during the power up sequence. Pin 9 is permanently tied to +5V and is unused during normal operation. The resistors R13 and R14 hold pins 8 and 10 low during power up and are large enough to allow the use of these pins as outputs during normal operation. The timing for the mode selection is shown in figure 4-8.

4.2.3.3 Power On/Off Reset

Refer to schematic 0103-00-1389, sheet 2. The power on/off reset circuit consists of three voltage comparators (U20A, U20C and U20D) and resistor voltage dividers to set thresholds. The comparator, U20D, controls the reset line ($\overline{MR}$) during power up and U20C controls the power off reset. The comparators have open collector outputs which can only pull their outputs low. The outputs are wire or'd together and pulled up by the resistor R4. When the instrument is turned on, the +5V supply pulls the voltage on the inverting input of U20D (pin 10) to a voltage determined by the voltage divider of R12, R8 and R6. The voltage on the noninverting input of U20D (pin 11) is pulled up at a much slower rate since the capacitor, C4 must be charged. While the voltage at pin 11 is lower than the voltage at pin 10 the comparator pulls $\overline{MR}$ low. Once C4 has charged to a voltage greater than the threshold on pin 10, $\overline{MR}$ is released and pulled high by R4. When the instrument is turned off the sequence is very similar. The +5V supply on the noninverting input of U20C (pin 9) drops rapidly while the voltage on the inverting input (pin 8) is held by the discharging C4, causing the comparator to pull $\overline{MR}$ low.

The comparator, U20A, controls the standby pin on the microprocessor. This line is held high by the resistor R3 during normal operation. When the instrument is turned off, the +5V supply on the noninverting input (pin 5) falls below the voltage on the inverting input (pin 4) set by the zener diode, CR1. This causes the comparator to pull $\overline{MR}$ low. The timing for the power on/off reset and standby control is shown in figure 4-8.

4.2.3.4 Address Decoder

Refer to schematic 0103-00-1389, sheet 2. All devices that interface with the microprocessor are assigned a unique address location. Devices that contain more than one location, memories for example, are assigned a block of addresses. When the microprocessor accesses a location, it outputs the 16 bit address of that location onto the address bus (ADR15-ADR0). It is the job of the address decoder to determine which location or block of locations is being accessed and enable that device. The address map in table 4-4 shows the address assignments for these peripheral devices.

The main components of the address decoder are three 1 of 8 decoders (U9, U13 and U27) and miscellaneous logic gates. Each decoder has three chip select inputs (pins 4,5 and 6) and three address select lines (pins 1,2 and 3). Of the chip select inputs, G1 must be high, and G2A and G2B low, to enable the decoder. When the decoder is enabled, the 3 bit binary number on its select lines determines which output is active. The Y7-Y0 outputs are active low.

Table 4-4. Microprocessor Address Map

Addressable Devices	Address (Hexadecimal)	Size
Internal Registers	$0000-$001F	32 bytes
Internal RAM	$0080-$00FF	128 bytes
Output Port 0	$0800	1 byte
Output Port 1	$0801	1 byte
Output Port 2	$0802	1 byte
Output Port 3	$0803	1 byte
Output Port 4	$0804	1 byte
Input Port 1	$0805	1 byte
Input Port 2	$0806	1 byte
RKIRQ (Reset Knob Interrupt)	$0807	1 byte
BC3 (Burst Count Read)	$0808	1 byte
BC2 (Burst Count Read)	$0810	1 byte
BC1 (Burst Count Read)	$0818	1 byte
Display	$0820-$0821	2 bytes
Communication Port	$1000-$1008	8 bytes
RAM	$2000-$3FFF	8K bytes
Waveform Memory	$4000-$7FFF	16K bytes
ROM	$8000-$FFFF	32K bytes

The most significant address line (ADR15), using the 'inverter' U2A, selects the 32K byte block containing the ROM. The combination of ADR15 and ADR14 are used by U2A and the 'nand' gate U3A to generate $\overline{\text{ARBMEM}}$ (U3A pin 3). This line is used to select the 16K byte block containing the waveform memory. The decoder, U13 uses the four most significant address lines to select either the main RAM, the communication option or one of the I/O ports of the microprocessor. When one of the I/O ports is selected, I/O (U13 pin 15) is low. This enables U9, which in conjunction with U27 further decodes the address into smaller blocks and selects individual lines or I/O devices. The "E" clock is used as one of the enable lines for U27 to synchronize data transfer between the microprocessor and the I/O devices.

4.2.3.5 Main Memory

Refer to schematic 0103-00-1389, sheet 2. The main memory section contains a read only memory (ROM) and a random access memory (RAM). The ROM (U31) contains 32,768 locations, each 8 bits wide and is the storage location for the instrument software. The software contains the instructions that drive the microprocessor. The RAM (U21) contains 8,192 locations, each 8 bits wide and is used to retain stored settings, and as a scratch pad and temporary data storage for the microprocessor.

When the microprocessor accesses the main memory, a read or write pulse must be generated to inform the the RAM and ROM of the type of cycle being executed. The "E" clock (U30 pin 40) and R/$\overline{\text{W}}$ (U30 pin 38) are gated together by the "nand" gate, U3B to produce the read pulse ($\overline{\text{RD}}$). This line pulses low when the microprocessor is ready to accept data during a read cycle. The write pulse is generated by gating $\overline{\text{R}}$/W and EB together at the "nand" gate U4B. The output of U4B (pin 6) goes low when the microprocessor is ready to output data during a write cycle.

When the ROM is accessed, the microprocessor outputs the 16 bit address (ADR15-ADR0) of the desired location. The lower 15 address lines (ADR14-ADR0) are used by the ROM to determine the location to be output. The address decoder section determines the memory block being accessed and pulls the chip enable (U31 pin 20) low. The ROM then puts the data stored in that location on the data bus (AD7-AD0) for the microprocessor to read.

The microprocessor can either read from or write to the RAM. To write data into the RAM, the write enable (pin 27) must be pulled low. To read data from the RAM the output enable (pin 20) must be pulled low. When the microprocessor accesses the RAM, the address of the desired location is put onto the address bus (ADR15-ADR0). The address decoder section pulls the chip select (RAM) on pin 20 of the RAM low. ADR12-ADR0 are used by the RAM to determine the location to be accessed. Depending on the type of cycle being executed, either the output enable (pin 22) or the write enable (pin 27) is pulled low and the data transfer takes place.

The RAM receives its power from the battery backed up supply (BBV). This allows the memory to retain the instrument setup when the power is turned off. While the instrument power is off, the RAM is still powered and its output enable (pin 22) is low. Unless it is disabled it will try to drive the data bus, consuming more power and draining the battery. The resistor, R17, and the analog switch, U1A, facilitate this by pulling the chip select line high when the power is off. During normal operation the reset line ($\overline{\text{MR}}$) is high and the switches in U1A are closed. When the instrument power is turned off, $\overline{\text{MR}}$ is pulled low by the power on/off reset circuit (ref: schematic 0103-00-1389 sheet 2) which opens the switches in U1A. The chip select for the RAM (U21 pin 20) is then pulled high through R17 and the memory is disabled.

4.2.3.6 Battery and Test Circuit

Refer to schematic 0103-00-1389, sheet 2. The main component of this circuit is a BR2/3A lithium battery (BT1). U20B is a voltage comparator used to test the battery voltage and interface to the microprocessor.

While the instrument power is turned on, the battery backed up supply (BBV) receives its power from the + 5V supply. Once the + 5V supply drops below the battery voltage, nominally + 3V, the power supplied to BBV is sourced by the battery. The diode, CR2, prevents the battery from discharging into the + 5V supply when the instrument power is turned off. CR3 prevents the + 5V supply from charging the battery while the instrument is turned on.

When the microprocessor tests the battery it pulls $\overline{\text{BLOAD}}$ low which places a slight load on it through the resistor R18. The battery voltage is then compared against the minimum threshold voltage set by R20 and R21. If the battery is good and its voltage is higher than the threshold, U20B pulls BTST (U20B pin 1) low. If the battery voltage is lower than the threshold, the resistor R23 pulls BTST high. This line is read by the microprocessor to determine the status of the battery. The microprocessor checks the battery when the instrument power is first turned on and at regular intervals during normal operation.

4.2.3.7 Front Panel and Front Panel Interface

Refer to schematic 0103-00-1389, sheets 1 and 3, and schematic 0103-00-1775. The front panel is the main interface between the user and the instrument.

It contains two sections, the keyboard and the display module. The circuitry on the keyboard interacts with the front panel interface and will be included in the discussion of that circuit. The display module however interfaces directly with the microprocessor.

The display module consists of a 16 character by 2 line liquid crystal dot matrix display with built in intelligent microprocessor bus interface. The microprocessor transfers data to and from the display module via its data bus, AD7-AD0 (J10 pins 14-7). When the microprocessor accesses the display module, the address decoder pulls $\overline{DISP}$ (U2B pin 3) low. This line is gated with the "E" clock by the 'and' gate U6B to create the display enable, DE (J10 pin 6). The data to be transferred is valid on the falling edge of DE. R/$\overline{W}$ (J10 pin 5) determines read or write cycles just as with any other microprocessor peripheral device. The microprocessor uses the least significant address line (ADR0) to select between the command register and the data register of the display drivers. The command register clears the display, moves the cursor, etc, while the data register selects the characters to be displayed.

The liquid crystal requires a DC drive voltage to provide its contrast. J10 pin 3 (DD) provides this voltage and is set by the LCD viewing control on the front panel. As this voltage changes, the intensity of the liquid crystal changes, essentially altering the optimum viewing angle. The resistors, R29 and R30 provide the biasing for the viewing angle control.

The front panel interface can be divided into two sections, the front panel keys and the control knob. There are eleven conductive rubber keys which interface to the microprocessor through two octal buffers (U32 and U33). These buffers act as input ports to the microprocessor data bus (AD7-AD0). The outputs of the buffers are in a high impedance state unless the enable on pins 1 and 19 is pulled low. The inputs to the buffers from the keys are pulled high by the resistor networks RN1 and RN2. When a key is pressed, it connects the buffer input to ground through the small key resistance. At regular intervals the microprocessor reads the keyboard input ports. When this happens the address decoder pulls the enable (IN0EN or IN1EN) of the appropriate buffer low and the data on the inputs is transferred to the microprocessor data bus.

An input to the Return In connector is routed to these input ports by the trigger and hold logic. This signal, $\overline{RTS}$ (U33 pin 4) is then treated as a key press.

The control knob on the front panel turns a conductive plastic rotary encoder. The encoder is constructed as two concentric striped conductive rings whose stripes are offset relative to each other. The conductive stripes are connected to ground. Each ring has a separate wiper (CPRE1 and CPRE2) which is pulled high through resistors R27 and R28. As the wiper contacts the stripe it is pulled low. As the shaft is rotated, two pulse trains, 90 degrees apart appear on the wipers. The phase difference between the wipers is either + 90 degrees or − 90 degrees depending on the direction of rotation.

The pulses from the encoder (CPRE1 and CPRE2) are interfaced to the microprocessor by a knob interrupt circuit. This circuit is comprised of the logic gates U34B, U34C, U8C, U35B, U35A, U10B, and U2E along with the transistor Q1. When the knob is rotated, one of the encoder lines changes state. This causes U2E pin 10 to go high which turns on Q1 and interrupts the microprocessor. When an interrupt occurs, $\overline{KIRQ}$ (U2E pin 11) goes low, latching IRQ (Q1 collector) low until the interrupt can be serviced. When the interrupt is serviced, the microprocessor reads the status of $\overline{KIRQ}$ (U33 pin 2) to determine if the knob was the source of the interrupt. If it was, the microprocessor compliments KM (U8C pin 5) which prohibits the knob input that just changed from causing another interrupt. This acts as a debounce and provides hysteresis for the knob inputs. The microprocessor also reads the status of CPRE1 and CPRE2 using the input port of U33. Based on the status of these lines, knob direction is calculated. The microprocessor writes the compliment of CPRE1 and CPRE2 to KW1 (U34B pin 4) and KW2 (U34C pin 10) respectively. This resets the inputs so that the next transition can be recognized by the circuit. After the interrupt has been serviced, the microprocessor pulses RKIRQ (U10B pin 3) low which sets IRQ (Q1 collector) high again and clears the knob interrupt circuit. The circuit is now ready to accept the next transition of the knob inputs.

4.2.3.8 Control Shift Register

Refer to schematic 0103-00-1456, sheet 2. The control shift register converts the serial data from the microprocessor to into 32 parallel control lines. These control lines direct the dedicated circuits for amplitude, offset and mode control, and the Z-Axis driver. The components of the circuit are; one triple 2-channel analog multiplexer (U11) and four 8 bit shift registers (U14, U13, U18 and U19).

The 8 bit shift registers are cascaded into a 32 bit serial to parallel converter. When the microprocessor writes to this circuit it sends a 32 bit serial string on the line SERD (U14 pin 2). With each bit the microprocessor pulses SERC (U14 pin 3) to clock the bit into the shift register.

As the data is shifted through the shift register, it carries out from pin 9 to the data input of the next register (pin 2). Once all 32 bits have been shifted in, the microprocessor pulses ANLE (U14 pin 1) high which transfers the new data to the outputs and latches it there.

The amplitude and offset control circuits (ref: schematic 0103-00-1456 sheet 4) must be driven with ± 5V logic levels. To accomplish this, three of the shift registers (U13, U18 and U19) are run on ± 5V power supplies. The multiplexer, U11, acts as a level shifter to change the normal 0 to 5V logic into ± 5V logic in order to properly drive U13, U18 and U19. U11 is actually three single pole double throw analog switches. One contact of each switch is connected to + 5V and the other contact is connected to − 5V. The wipers of each switch appear at pins 14, 15 and 4. The data line (SERD), clock line (SERC) and the enable (ANLE) are connected to the control pins for the switches (pins 9, 10 and 11). When the control pin is low, the wiper of the switch is connected to the − 5V contact causing a logic low output. When the control pin is high, the wiper is connected to the + 5V contact causing a logic high output.

4.2.3.9 Output Ports

Refer to schematic 0103-00-1389, sheets 2 and 4. The output ports provide a parallel interface from the microprocessor to the dedicated circuits. The output ports can be divided into two blocks, the burst counter preload and the start address preload. The output ports are driven by the latched data bus (LDB7-LDB0). The latched data bus is created by the octal transparent latch (U46). The microprocessor's data bus is connected to the inputs of U46 (pins 3,4,7,8,13,14,17 and 18). The "E" clock is connected to the clock input of U46 (pin 11). When the data on the data bus (AD7-AD0) is valid, the "E" clock goes low and the data is latched into the outputs of U46. The purpose of this latch is to reduce loading on the microprocessor data bus and to improve the hold time of the data for the output ports.

The burst counter preload (ref: schematic 0103-00-1389 sheet 4) provides a 20 bit binary number for the burst counter. It consists of three octal D type flip flops (U49, U45 and U39). The start address preload (ref: schematic 0103-00-1389 sheet 2) provides the 13 bit waveform start address to the waveform address counter. It is comprised of two of the same type of octal flip flops (U26 and U22). In both circuit blocks, the information present on the D inputs of the latches (pins 3,4,7,8,13,14,17 and 18) is transferred to the Q outputs (pins 2,5,6,9,12,15,16 and 19) on the rising edge of the clock input (pin 11). When the microprocessor writes to one of the output ports, it places the data on its data bus (AD7-AD0) where it is latched by U46. The address decoder selects which output port is being addressed and pulls the appropriate enable (U27 pins 15-11) low. When the enable is released, the data is latched into the output port and is available for the dedicated circuit.

Besides the control busses mentioned above, the output ports also supply 6 individual control lines. On U26, are three lines ($\overline{\text{PLOAD}}$, PCLK, and $\overline{\text{SELOVR}}$) that are used during a return to start. On U39, are three lines (SLOPE, $\overline{\text{MANHOLD}}$ and $\overline{\text{TRIGGERMASK}}$) that are used in the trigger and hold logic.

4.2.4 Communication Options

4.2.4.1 General Description

The communication options provide a means for the user to enter and query instrument parameters and waveform information via an external computer or instrument controller. Either an IEEE-488 parallel interface (option 001) or a RS-232-C serial interface (option 002) may be installed.

4.2.4.2 IEEE-488 (Option 001)

Refer to schematic 0103-00-1678. The IEEE-488 option, also referred to as GPIB (general purpose interface bus) consists of a general purpose interface adapter (U2), two bus transceivers (U3 and U4), one hex buffer (U1) and one 5 position SPST switch (SW1). All GPIB data transfers and bus protocols are handled by the general purpose interface adapter (GPIA). This device transfers data to and from the bus via U3. The control lines are interfaced to the bus through U4. These transceivers handle the driving capability and line termination requirements for the GPIB bus and are enabled when the GPIA sets their pin 1 high. For an explanation of the data and control lines refer to Section 3.27.

The GPIA (U2) contains a data in register, a data out register and several control registers. Information is transferred between these registers and the microprocessor via the microprocessor data bus (U2 pins 14-7). The microprocessor section enables the GPIA by pulling $\overline{\text{COMM}}$ low (U2 pin 3). The data transfer is synchronized by the "E" clock on U2 pin 6. This is a 1 MHz clock that originates in the microprocessor section. R/$\overline{\text{W}}$ on U2 pin 5 is the read/write control from the microprocessor. The microprocessor selects which register is accessed with the three least significant address lines (U2 pins 37, 38 and 39). When the GPIA needs the attention of the microprocessor, it pulls $\overline{\text{IRQ}}$ (pin 40) low. This causes the microprocessor to execute an interrupt service routine which interrogates the GPIA and transfers the necessary information. Pin 19 of the GPIA is connected to the master reset line ($\overline{\text{MR}}$). When the instrument power is turned on, this line goes low and forces the GPIA into a reset condition.

When the instrument power is turned on, the microprocessor executes an initialization routine for the GPIA. As part of this routine, an address switch register is

accessed. When this occurs the GPIA sets its address switch enable line (U2 pin 4) low. This causes the buffer, U1, to transfer the address, as set by SW1, to the microprocessor data bus. The microprocessor then writes this address into an address register in the GPIA. For more information on the GPIB address, refer to Section 2.2.6.

4.2.4.3 RS-232-C (Option 002)

Refer to schematic 0103-00-1677. The RS-232-C option consists of an asynchronous communication interface adapter (U1), a baud rate generator (U2), a quad line driver (U3), a quad line receiver (U4) and a 5 position SPST switch (SW1). The asynchronous communication interface adapter (ACIA) interfaces between the parallel communication of the microprocessor section and the asynchronous serial communication of the RS-232 interface. All RS-232 transactions are handled by the ACIA which alerts the microprocessor when it needs attention.

Data and control lines that are output to the interface are driven by U3. This line driver inverts and translates the TTL logic levels from the ACIA to ±12V (nominal) logic that meets the RS-232 specifications. The capacitors, C7 and C9, reduce the slew rate of the outputs to meet RS-232 specifications. Data and control lines that are input from the bus are received by U4. This line receiver translates and inverts the widely varying logic levels from the bus, into TTL logic levels for the ACIA. Any input between +3V and +25V is detected as a logic "0" and between −3V and −25V is a logic "1". The capacitors C8, C10 and C11 act as noise filters for the inputs. For a detailed description of the RS-232 signals refer to Sections 2.2.7 and 3.31.

The baud rate of the transmitted data is determined by the frequency input to pins 3 and 4 of U1, which is 16 times the baud rate. The source of this frequency is the baud rate generator U2. U2 has an internal oscillator whose frequency is based on the 2.4576 Mhz crystal, Y1. Using internal dividers, the output frequency of U2 can be set to one of 14 frequencies with SW1 switches 1 thru 4. Table 2-4 shows the baud rate switch settings.

The ACIA contains internal registers for transmit data, receive data, status and control. Of these registers, transmit data and control are write only and the others are read only. These registers are accessed by the microprocessor via the data bus AD7-AD0 (U1 pins 15-22). The microprocessor section enables the ACIA by setting $\overline{\text{COMM}}$ (U1 pin 9) low. The least significant address line (ADR0) drives the register select pin of U1 (pin 11). This line selects either the transmit/receive data registers when high or the control/status registers when low. The microprocessor read/write control (U1 pin 13) is used in conjunction with the register select to select the read only or write only register of each pair. The "E" clock (U1 pin 14) from the microprocessor synchronizes the data transfer. When the ACIA needs attention from the microprocessor it pulls $\overline{\text{IRQ}}$ (U1 pin 7) low. The microprocessor then executes an interrupt service routine which reads the status register and performs the necessary data transfer.

4.2.5 Power Supply

4.2.5.1 General Description

Three DC power supply voltages are generated on the power supply circuit board; ±15V and +5V. These voltages are generated from either 115Vac or 230Vac line as selected by the user. See section 2.2.3 for line voltage information.

4.2.5.2 +5V Power Supply

Refer to schematic 0103-00-1113. AC voltage from the transformer, T1, is rectified by the diode bridge CR2 and filtered by the capacitors C10 and C11. This provides an unregulated DC voltage for the +5V regulator VR2. The capacitor, C12 provides filtering of high frequency noise and insures the stability of VR2. The capacitor, C9 protects against high voltage transients on the AC line that couple onto the transformer secondary.

4.2.5.3 ±15V Power Supply

Refer to schematic 0103-00-1113. The transformer, T1 provides an AC voltage with a ground referenced center tap. This voltage is rectified by the diode bridge CR1 and filtered by the capacitors C2, C3, C4 and C5. This provides unregulated ± DC voltages for the regulator VR1. The capacitor, C1 protects against high voltage transients on the AC line that couple onto the transformer secondary. For the +15V supply, VR1 senses the output voltage at pin 14 and modulates the base of the pass device, Q1, thus regulating the output voltage. The capacitors, C6 and C8, provide filtering at the regulator output. The load current causes a voltage drop across the resistor, R2. When the load current reaches its limit, the regulator senses the drop across R2 and reduces the output voltage until the current falls below the limiting value. The −15V supply operates in a similar manner and tracks the +15V supply.

SECTION 5
CALIBRATION

5.1 SCOPE

This section gives the procedures to be used for the calibration and specification verification of the Model 75. Complete instrument specifications are given in Section 1 of this manual. For a complete functional verification, refer to Section 2.3.

5.2 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize the turnaround time.

5.3 REQUIRED TEST EQUIPMENT

The test equipment required to perform the calibration procedures given in paragraphs 5.4 through 5.9 is listed in table 5-1.

5.4 CALIBRATION

Calibration of the Model 75 is performed solely through the use of front panel controls. Allow the instrument to warm up at least 30 minutes before beginning calibration. Do not remove instrument covers during this procedure. Once the calibration has been performed, the instrument will hold calibration as long as the internal battery maintains the memory. If the display indicates Wavetek Model 75 "Cold Start" on power up, the memory has been lost and the following calibration steps must be performed.

1. Interconnect the Model 75 and test equipment as shown in figure 5-1.
2. Set the digital voltmeter (DVM) as follows:

Function	DC Volts
Resolution	Maximum

3. Perform the steps in the order shown in table 5-2.

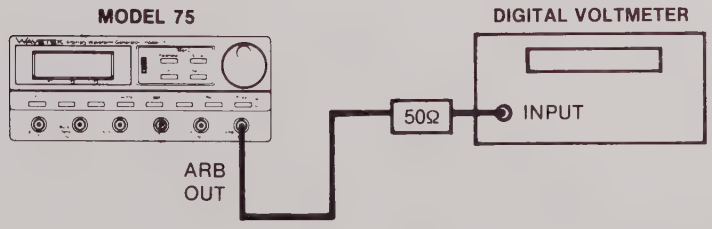


Figure 5-1. Calibration Equipment Connection

Table 5-1. Required Test Equipment

Equipment	Quantity	Specifications
Oscilloscope.	1	Dual channel, ⩾ 20 MHz bandwidth and external trigger input.
50Ω Termination.	1	Feedthrough, 0.1% accuracy, 2W.
50Ω Termination.	1	Feedthrough, 5% accuracy, 2W, carbon element. (For use in paragraph 5.8 only.)
BNC Tee	1	1 male to 2 female connection.
Signal Source	1	Capable of 1 MHz TTL and 10 Vp-p sine wave (into 50Ω).
Frequency Counter	1	6½ digit resolution and period measurement capability.
Digital Voltmeter (DVM)	1	4½ digit resolution.
Coaxial Cables	4	BNC male connectors, RG-58U cable.

Table 5-2. Calibration Procedures

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values. Verify that "RESET (VER x.xx)X" appears on the display.
2. Edit, ERASE (F2), EXEC (F3)	Clears waveform memory.
3. Parameter, AMPL (F1), Control knob	Set the amplitude to 2.500 Vp.
4. Setup, CAL (F3), Control knob	Adjust the knob until the reading on the DVM is $< \pm 3$ mV. The number that appears in the display is the CAL constant. Press any other menu key to lock in the CAL constant value.
5. Parameter, AMPL (F1), Control knob	Set the amplitude to 5.000 Vp. This returns the instrument to the normal setup amplitude value.

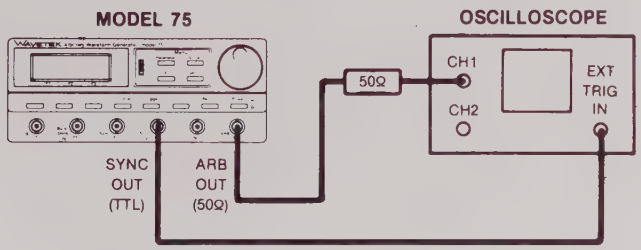


Figure 5-2. Amplitude Verification Equipment Connection

5.5 AMPLITUDE

This paragraph verifies the waveform amplitude accuracy of the Model 75 throughout its range. If the readings are outside the upper or lower limits, perform the steps given in paragraph 5.4 (Calibration) and then recheck using this paragraph. If the instrument still fails to fall within specifications, refer to Section 6 (Troubleshooting) and Section 4 (Circuit Description) for help in solving the problem.

1. Interconnect the Model 75 and test equipment as shown in figure 5-2.
2. Set the oscilloscope controls as follows:

Vertical Input	CHAN 1
Vertical Gain	2V/DIV
TIMEBASE	0.5 ms/DIV
Trig Source	External

3. Perform the steps in the order shown in table 5-3.

Table 5-3. Amplitude Verification

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values.
2. Edit, ERASE (F2), EXEC (F3)	Clears waveform memory.
3. Edit, FUNC (F1), Control knob	Rotate to select FUNC SINE.
4. EXEC (F3)	Verify a sine wave of slightly more than 2 cycles and approximately 10 Vp-p in amplitude.
5. Parameter, AMPL (F1), Control knob	Adjust the amplitude from 5.000 Vp down to 5.00 mVp. Verify that the waveform amplitude decreases smoothly to 10 mVp-p.
6. Control knob	Set the amplitude to 25.00 mVp.
7. Connect the ARB OUT connector to the DVM and terminate cable with 50Ω at the DVM input. Set the DVM to the "dc volts" function and for maximum resolution.	

Table 5-3. Amplitude Verification (Cont)

Press/Adjust	Remarks
8. Edit, STOP (F2), Control knob	Set the STOP address (SP) to 0000.
9. Edit, ADJX,Y (F2), Control knob	Adjust the "Y" value to "Y = 2047". Record the DVM reading.
10. Control knob	Adjust the "Y" value to "Y = −2047". Record the DVM reading.
11. Add the magnitudes of both the positive and the negative readings together for the peak to peak amplitude value and record.	
12. Parameter, AMPL (F1), Control knob	Repeat steps 9, 10 and 11 for each of the following amplitude settings. Verify that the peak to peak amplitudes are within the specified limits.

SETTING	UPPER LIMIT	LOWER LIMIT
25.00 mVp	50.95 mVp-p	49.05 mVp-p
250.0 mVp	509.5 mVp-p	490.5 mVp-p
0.500 Vp	1.023 Vp-p	0.9770 Vp-p
2.500 Vp	5.095 Vp-p	4.905 Vp-p
5.000 Vp	10.185 Vp-p	9.815 Vp-p

5.6 OFFSET

This paragraph verifies the dc offset accuracy of the Model 75 throughout its range. If the readings are outside the upper or lower limits, perform the steps given in paragraph 5.4 (Calibration) and then recheck using this paragraph. If the instrument still fails to fall within specifications, refer to Section 6 (Troubleshooting) and Section 4 (Circuit Description) for help in solving the problem.

1. Interconnect the Model 75 and test equipment as shown in figure 5-3.

2. Set the digital voltmeter (DVM) as follows:

Function	DC Volts
Resolution	Maximum

3. Perform the steps in the order shown in table 5-4.

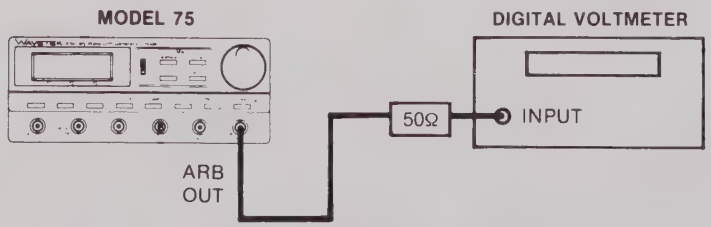


Figure 5-3. Offset Verification Equipment Connection

Table 5-4. Offset Vertification Procedures

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values.
2. Edit, ERASE (F2), EXEC (F3)	Clears waveform memory. Verify that the ARB OUT offset value as shown on the DVM is 0V ±5 mV.
3. Parameter, AMPL (F1), Control knob	Set amplitude to 5.00 mVp.
4. OFFSET (F2), Control knob	Adjust the offset to each of the following settings. Verify that the DVM offset values are within the specified limits for each setting.

SETTING	UPPER LIMIT	LOWER LIMIT
5.00V	5.115V	4.885V
0.50V	0.5250V	0.4750V
495 mV	519.9 mV	470.1 mV
45 mV	47.40 mV	42.60 mV
44.9 mV	45.95 mV	43.85 mV
−44.9 mV	−43.85 mV	−45.95 mV
−45 mV	−42.60 mV	−47.40 mV
−495 mV	−470.1 mV	−519.9 mV
−0.50V	−0.4750V	−0.5250V
−5.00V	−4.885V	−5.115V

5. Remove the ARB OUT cable with the 50Ω termination from the DVM and connect to the oscilloscope CHAN 1 vertical input.	
6. Control knob	Adjust the offset from −5.00V to +5.00V and verify that the output level smoothly increases from −5V to +5V.

5.7 FREQUENCY

This paragraph verifies the sample frequency accuracy of the Model 75 throughout its range. If the readings are outside the upper or lower limits, the instrument is in need of repair. Refer to Section 6 (Troubleshooting) and Section 4 (Circuit Description) for help in solving an out of tolerance problem.

1. Interconnect the Model 75 and test equipment as shown in figure 5-4.
2. Set the frequency counter controls to measure frequency with maximum resolution.
3. Perform the steps in the order shown in table 5-5.

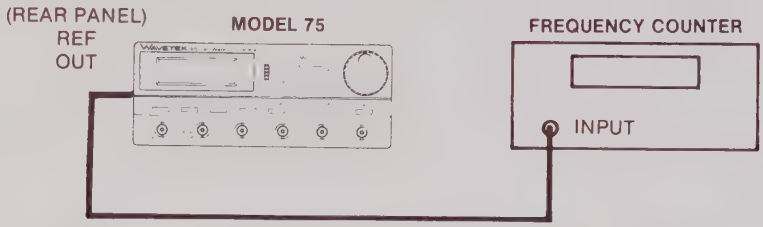


Figure 5-4. Frequency Verification Equipment Connection

Table 5-5. Frequency Verification

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values.
2. Parameter, SAMPL (F2), Control knob	Set the sample frequency to each of the settings given in table 5-6. Verify on the frequency counter that each frequency setting falls within the upper and lower limits given in the table.

Table 5-6. Frequency Verification Limits

SETTING	UPPER LIMIT	LOWER LIMIT
1.0000 MHz	1.000150 MHz	0.999850 MHz
500.0 kHz	500.050 kHz	499.925 kHz
300.0 kHz	300.045 kHz	299.955 kHz
100.0 kHz	100.0150 kHz	99.9850 kHz
10.000 kHz	10.00150 kHz	9.99850 kHz
1.000 kHz	1.000150 kHz	0.999850 kHz
100.0 Hz	100.0150 Hz	99.9850 Hz
NOTE: Set the frequency counter to measure period.		
10.000 Hz	100.0150 ms	99.9850 ms
1.0000 Hz	1.000150 s	0.999850 s
100.0 mHz	10.00150 s	9.998500 s

5.8 OUTPUT WAVEFORM RISE AND FALL TIME

This paragraph verifies that the rise and fall time of the Model 75 output waveform falls within the specified limits. If the readings are outside the specified limits, perform the steps given in paragraph 5.4 (Calibration) and then recheck using this paragraph. If the instrument still fails to fall within specifications, refer to Section 6 (Troubleshooting) and Section 4 (Circuit Description) for help in solving the out of tolerance problem.

1. Interconnect the Model 75 and test equipment as shown in figure 5-5. Use the 50Ω termination with the carbon element in this step.
2. Set the oscilloscope controls as follows:

Vertical Input	CHAN 1
Vertical Gain	2V/DIV
TIMEBASE	0.2 μs/DIV
Trig Source	External

3. Perform the steps in the order shown in table 5-7.

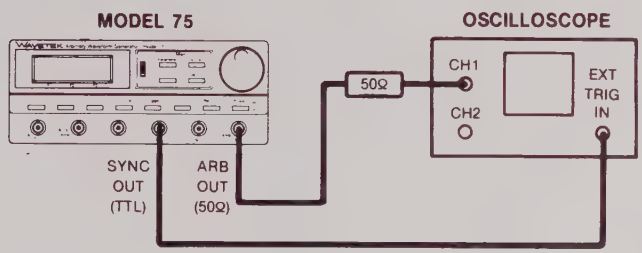


Figure 5-5. Output Waveform Verification Equipment Connection

Table 5-7. Output Waveform Rise/Fall Time Verification

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values.
2. Edit, ERASE (F2), EXEC (F3)	Clears waveform memory.
3. Edit, STOP (F2), Control knob	Set the STOP address to "0001".
4. Edit, L,RTT (F3), Control knob	Set the right thumb tack (R) to "0001".
5. Edit, FUNC (F1), Control knob	Select FUNC SQUARE.
6. EXEC (F3)	Verify that the rise and fall times (from 10% to 90% of full transition) are < 350 ns. Verify that any aberrations (ringing and/or overshoot) on the waveform are < 300 mVp-p.

5.9 SUM IN

This paragraph verifies that the "Sum In" gain accuracy of the Model 75 falls within the specified limits. If the instrument fails to fall within specifications, refer to Section 6 (Troubleshooting) and Section 4 (Circuit Description) for help in solving the problem.

1. Interconnect the Model 75 and test equipment as shown in figure 5-6.
2. Set the oscilloscope and Signal Source controls as follows:

Digital Voltmeter		Signal Source	
Function	AC Volts	Output Freq	1 kHz
		Output Amplitude	10 Vp-p

3. Perform the steps in the order shown in table 5-8.

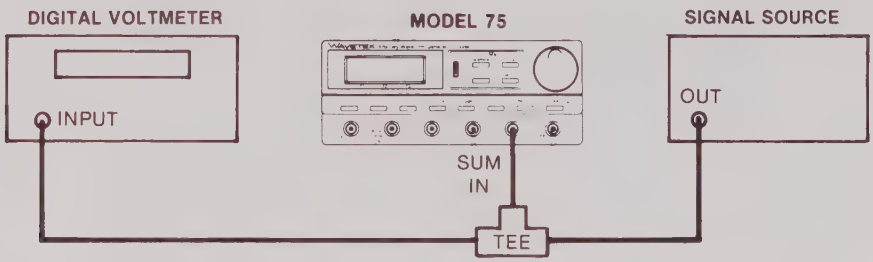


Figure 5-6. SUM IN Verification Equipment Connection

Table 5-8. Output Waveform Rise/Fall Time Verification

Press/Adjust	Remarks
1. Setup, RSET (F2), EXEC (F3)	Sets default values.
2. Edit, ERASE (F2), EXEC (F3)	Clears waveform memory. Record the DVM reading.
3. Disconnect the input signal to DVM. Connect the Model 75 ARB OUT connector to the DVM terminated into 50Ω.	
4.	Record the DVM reading. Verify that the input to output error is <4%.

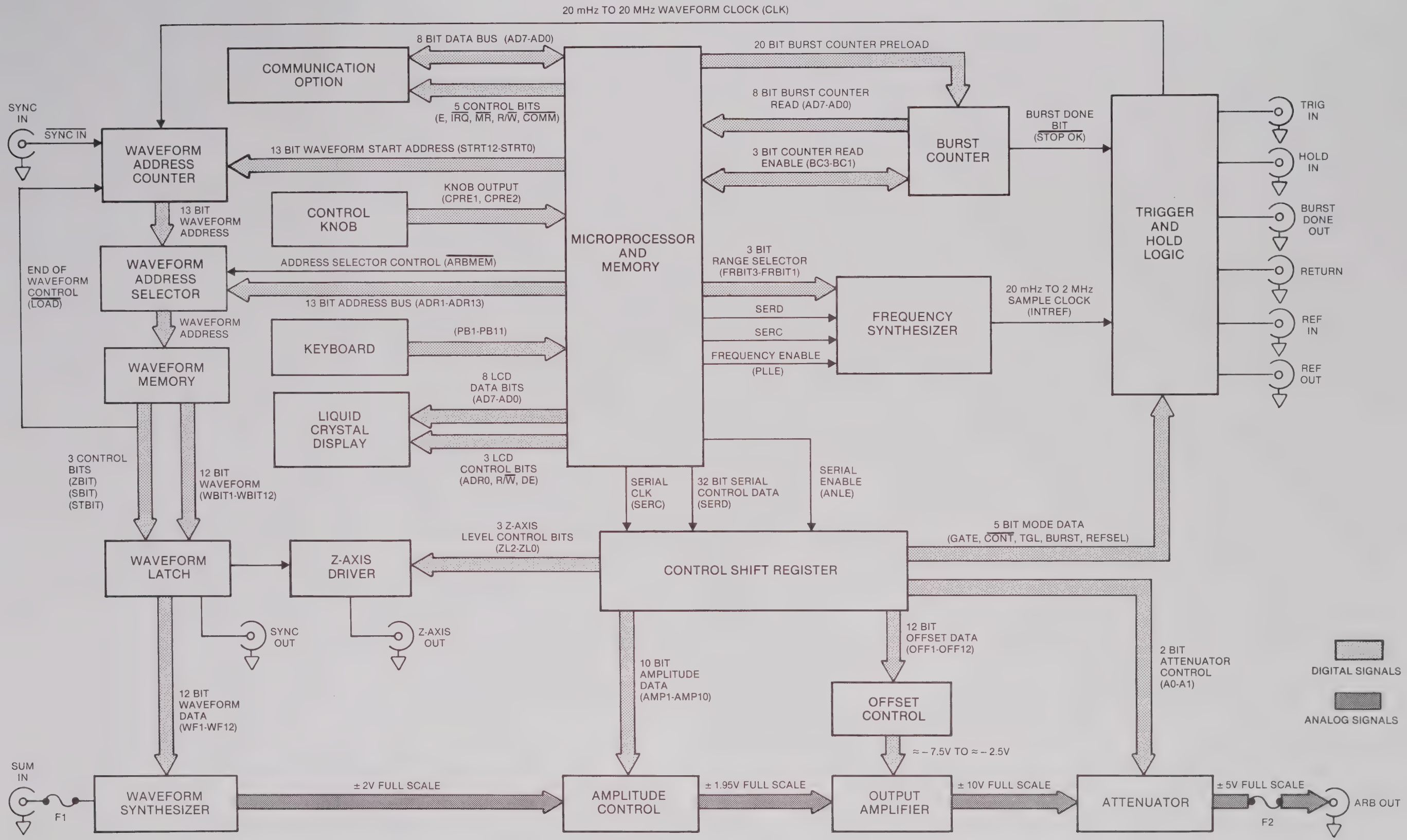


Figure 6-1. **Troubleshooting Block Diagram**

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description (Section 4) in conjunction with the schematics (Section 7). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

The intent of this section is to provide the information required to return this instrument to proper operation. Information is divided into two parts. Part one contains the overall instrument troubleshooting block diagram (figure 6-1), which is useful in isolating defective blocks within the instrument. Part two consists of a series of circuit guides (table 6-1), one for each block shown in figure 6-1, that provides settings and measurements for troubleshooting an individual block. Also, each circuit guide references related schematics, circuit descriptions, and calibration procedures.

Before beginning the troubleshooting process, verify that the instrument's controls are set correctly. Table 6-2 gives examples of possible symptoms that can be the result of a setup error. For more information about the instrument controls and operation, refer to Section 3 of this manual.

Inspect the instrument's components, wiring and circuit boards for damage. Finally, ensure that the ac fuse is intact and the internal dc power supplies, ±15 Vdc, ±5 Vdc, and +10 Vdc, are good.

6.2.1 Isolating a Problem

To successfully troubleshoot this instrument, the symptom must first be identified, the faulty block isolated, the block analyzed, and the defective component located and replaced.

To identify the symptom, use all of the front panel controls and connectors. For example, if the sample frequency control is not working, are any other parameter controls defective?

Once the symptom is identified, use figure 6-1 to isolate the circuit block. After the block is isolated, refer to the appropriate functional circuit guide (table 6-1).

The circuit guides provide some but not necessarily all of the possible failure modes for a particular circuit. Where applicable, an instrument setup is given to help isolate the problem for a particular failure mode. Paragraph 6.4 gives component troubleshooting information.

NOTE

In the following tables, an expression like "U33-5" refers to pin 5 of integrated circuit U33. All pins on referenced integrated circuits and connectors are referred to in the same manner.

Table 6-1. Functional Circuit Guides

Circuit Guide	Paragraph: Circuit Description (4.X) Calibration (5.X) Troubleshooting(6.X)			Troubleshooting Tables	Schematic Diagrams
Power Supply	4.2.5		6.3.1	6-3, 6-4	0103-00-1113
Frequency Synthesizer	4.2.2.2			6-5, 6-6, 6-7	0103-00-1456
Trigger and Hold Logic	4.2.2.3			6-8, 6-9	0103-00-1456
Waveform Address Counter	4.2.1.2			6-10	0103-00-1389
Waveform Memory	4.2.1.4			6-11	0103-00-1389
Waveform Latch	4.2.1.5			6-12	0103-00-1456
Waveform Synthesizer	4.2.1.6	5.4		6-13, 6-14	0103-00-1456
Amplitude Control	4.2.1.7	5.4		6-15	0103-00-1456
Offset Control	4.2.1.8	5.4		6-16	0103-00-1456
Output Amplifier	4.2.1.9			6-17	0103-00-1456
Attenuator	4.2.1.10			6-18	0103-00-1456
Burst Counter	4.2.2.4			6-19	0103-00-1389
Control Shift Register	4.2.3.8			6-20	0103-00-1456
Z-Axis Driver	4.2.1.12			6-21, 6-22	0103-00-1456
Keyboard	4.2.3.7			6-23	0103-00-1775 0103-00-1389
Control Knob	4.2.3.7			6-24	0103-00-1775 0103-00-1389
Liquid Crystal Display	4.2.3.7			6-25	0103-00-1775 0103-00-1389
Microprocessor and Main Memory	4.2.3		6.3.2	6-26	0103-00-1389
Communication Option 001:GPIB	4.2.4.2			6-27	0103-00-1678
Communication Option 002:RS-232	4.2.4.3			6-28, 6-29	0103-00-1677

Table 6-2. Instrument Setup Common Errors

Symptom	Possible Setup Error
Display blank.	LCD viewing angle misadjusted.
No Output.	Hold Key "On". Mode not set to "Continuous". Start Adrs equals Stop Adrs. External reference selected with no reference connected to Ref In connector. DC waveform selected.
Runs continuously in triggered, gated, toggled or burst modes.	No "breakpoints" set.

Symptom	Possible Setup Error
The following apply only to instruments with the communications option installed.	
No response from the Control knob.	Unit set for remote operation.
No response to RS-232-C control.	Baud rate set incorrectly (refer to section 2.2.7). Not configured properly; DCE or DTE (refer to section 2.2.7).
No response to IEEE-488 control.	Instrument address set incorrectly (refer to section 2.2.6).

6.2.2 Troubleshooting Dynamic Digital Circuits

Most of the digital circuits in this instrument are dynamic. Even with no changes made to the instrument setup, internal circuits are running and lines are changing states. This makes troubleshooting difficult without the use of powerful tools, a logic analyzer for instance.

There is, however, a technique using an oscilloscope which will usually help isolate an abnormal signal. The basis of this technique is looking for stuck bits. A normal digital signal will switch between a logical "1" (a high) and a logical "0" (a low). A stuck bit may not switch at all. It may be always high, always low, or always between logic levels in an undefined state. A stuck bit may also switch between high or low levels and the undefined state. Figure 6-2 shows examples of good dynamic digital signals and figure 6-3 gives examples of stuck bits.

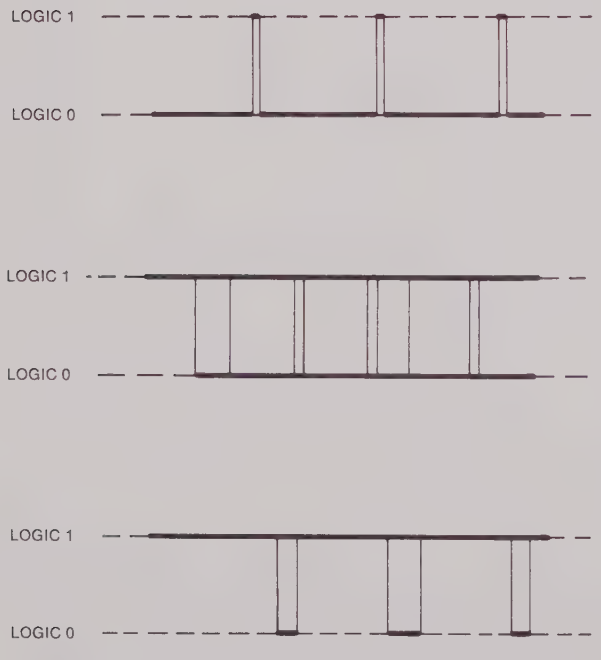


Figure 6-2. Normal Digital Signals

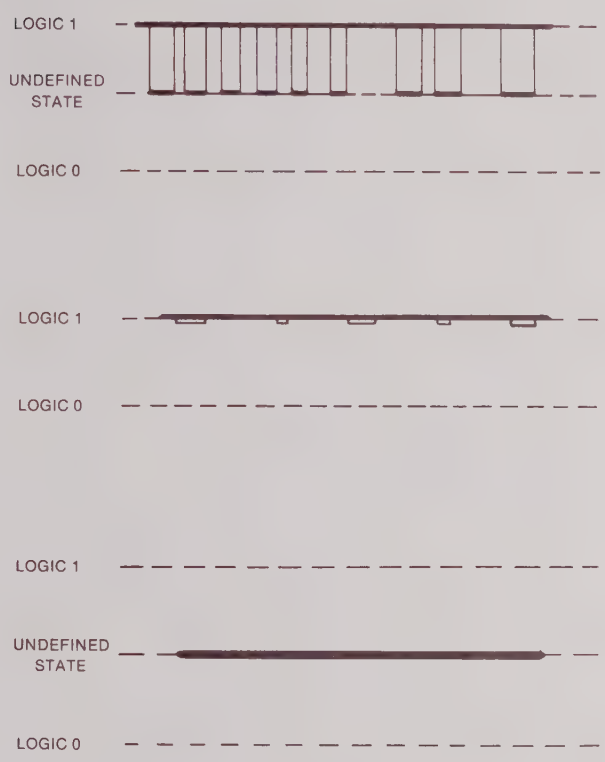


Figure 6-3. Defective (Stuck Bits) Digital Signals

6.3 TROUBLESHOOTING GUIDES

Refer to table 6-1 for circuit guide information.

6.3.1 Power Supply

To determine a faulty power supply use table 6-3. To troubleshoot a faulty power supply use the procedures listed in table 6-4. For fuse replacement, refer to paragraph 2.2.3.

If the desired results are obtained in each of the steps in table 6-4, replace either Q1, Q2, VR1, or VR2 as appropriate.

Table 6-3. Power Supply Voltages

Output Voltage	Voltage Tolerance	Output Ripple (Max)	Test At	Input Ripple (Max)	Test At
+5V	±250 mV	0.02 Vac	C12	3 Vac	C10
+15V	±350 mV	0.02 Vac	C7	3 Vac	C2
−15V	±350 mV	0.02 Vac	C8	3 Vac	C3

Table 6-4. Power Supply Troubleshooting

Fault	Setup	Check	Results Desired
No dc output and no dc to C2/C3 (±15V) or C10 (+5V)	Power off	F1	<1 ohm
		T1 windings	Not shorted or open.
		CR1 (±15V) or CR2 (+5V)	Not shorted or open.
		C2, C3, C4, C5, (±15V) or C10 and C11 (+5V)	Not shorted.
		Q1, Q2, VR2 tabs	Not shorted to frame or ground.
Low or no dc output and dc to C2/C3 (±15V) or C10 (+5V) is slightly low or normal.	Power off. Disconnect J4 and J5. Power on	P4 and P5	If all voltages normal, check for excessive loading
	Power off	C6, C7, C8 (±15V) or C12 (+5V)	Not shorted.

Table 6-5. Frequency Synthesizer Troubleshooting

Fault	Setup	Check	Results Desired
No sample clock (INTREF).	Reset	U36-6 U31-8 (VCO output) U37-6 (PLL output) U29-5 (divider out) U28B-9 (INTREF)	6.144 MHz 5 MHz 5 MHz 5 MHz 1 MHz
Sample frequency not at setting.	Reset	Pins on U29 and U36 as shown in table 6-6 and 6-7.	Bit levels as shown in table 6-6 and 6-7.

Table 6-6. Frequency Ranging

NOTE: (1 = high, 0 = low)

Sample Frequency Range	FRBIT1 U29-9	FRBIT2 U29-10	FRBIT3 U29-11
2 MHz – 200 kHz	1	1	1
199.98 kHz – 20 kHz	1	1	0
19.998 kHz – 2 kHz	1	0	1
1.9998 kHz – 200 Hz	1	0	0
199.98 Hz – 20 Hz	0	1	1
19.998 Hz – 2 Hz	0	1	0
1.9998 Hz – 200 mHz	0	0	1
199.98 mHz – 20 mHz	0	0	0

Table 6-7. Inner-range Switching

Display Counts	SW1 U36-13	SW2 U36-14	VCO Frequency U31-8
19998 – 16000	1	1	9.999 MHz – 8.000 MHz
15998 – 8000	1	0	7.999 MHz – 4.000 MHz
7998 – 4000	0	1	7.998 MHz – 4.000 MHz
3998 – 2000	0	0	7.996 MHz – 4.000 MHz
2.000 MHz	1	1	10.000 MHz

Table 6-8. Trigger and Hold Logic Troubleshooting

Fault	Setup	Check	Results Desired
Sync In (external) not functional.	Reset. Apply 1 kHz TTL signal to Sync In connector.	U21A-3	Inverted version of input signal.
Hold In (ext) or hold key not functional.	Reset. Press Hold key. Release Hold key. Apply TTL low to Hold In connector.	U27B-6 U27B-6 U27B-6	A TTL high. A TTL low. A TTL low.

Table 6-8. Trigger and Hold Logic Troubleshooting (Cont)

Fault	Setup	Check	Results Desired
Ref In (ext) not functional.	Reset. Apply 100 kHz TTL signal to Ref In connector. Select Ext reference.	 U12D-8 U21C-8	 A 100 kHz signal. A 100 kHz signal.
Trig In (ext) not functional or Manual trigger not functional.	Reset. Select triggered mode. Set sample frequency to 100 kHz.	 U15B-5 U15B-6 U23B-8 U15B-5	 A high. A low. Pulses low when TTL high applied to Trig In connector. Low when trigger key is pressed.
Ref Out (int) not functional.	Reset.	U25F-13 U25F-12	A 1 MHz TTL signal. An inverted version of signal at U25-13.
Burst Done Out (Int) not functional.	Reset.	U25B-3	A high with a low going pulse every 2 ms.
Return In (ext) not functional.	Reset. Apply TTL low to Return In connector. Remove input from Return In connector.	 U12E-10 U12E-10	 A TTL high. Is now low.
Return In and return key not functional.	Reset. Select Ramp Up function. Press Return key.	 U15D-13	 A high with low going pulses every 5 ms during the return ramp.
No waveform clock (CLK)	Reset.	U25D pin 9 U25E pin 11 U15A pin 3 U27C pin 8 U22A pin 12 U15D pin 11	1 MHz TTL high 1 MHz TTL high TTL high 1 MHz
Trigger, gated, toggle, or burst modes not functioning.	Reset. Select modes indicated and take measurements shown in table 6-9.		

Table 6-9. Mode Control

Mode	Cont/ U23B-10	Gate U21B-4	TGL U15C-9	Burst U21D-12
Continuous	Low	Low	Low	Low
Triggered	High	Low	Low	Low
Gated	High	High	Low	Low
Toggled	High	High	High	Low
Burst	High	Low	Low	High

Table 6-10. Waveform Address Counter Troubleshooting

Fault	Setup	Check	Results Desired
Waveform data is static. Waveform stop address not functioning properly.	Reset. Set stop address to 10.	U24-2. U35C-11 U35C-10 U10C-10 U4C-8 U24-14.	A 1 MHz signal. A TTL high. A Low. A TTL High. A TTL high with 1 μs wide low going pulse every 11 ms. 500 kHz held low for approximately 2 μs coincident with load pulse (U4-8).
	Set stop address to 8191.	A0 (U24-14) A1 (U24-13) A2 (U24-12) A3 (U24-11) A4 (U25-14) A5 (U25-13) A6 (U25-12) A7 (U25-11) A8 (U28-14) A9 (U28-13) A10 (U28-12) A11 (U28-11) A12 (U36-14) U29-1	500 kHz 250 kHz 125 kHz 62.5 kHz 31.25 kHz 15.625 kHz 7.813 kHz 3.906 kHz 1.953 kHz 977 Hz 488 Hz 244 Hz 122 Hz A high
	Adjust waveform editing cursor.	U29-1.	Low going pulses.
Waveform start address not functioning properly.	Reset.	U35C-10 U35C-11 U10C-10 U36-3 U28-3 thru -6 U25-3 thru -6 U24-3 thru -6	A Low A TTL high A TTL High A Low All are low. All are low. All are low.

Table 6-10. Waveform Address Counter Troubleshooting (Cont)

Fault	Setup	Check	Results Desired
	NOTE *Set the start address to various settings and verify that its binary value appears on STRT12 thru STRT0. STRT0 is the least significant byte. An example is "Start address = 1000, STRT12 thru STRT0 = 001111101000".*		
	Apply TTL high to Sync In connector.	U36-14 U28-11 thru -14. U25-11 thru -14. U24-11 thru -14.	Same as STRT12 Same as STRT11-STRT8 Same as STRT7-STRT4 Same as STRT3-STRT0
"Return In" and Return key not functioning.	Reset. Select Ramp Up function. Press Return key.	U10C-10	A TTL high with low going pulses every 5 ms during the return ramp.

Table 6-11. Waveform Memory Troubleshooting

Fault	Setup	Check	Results Desired
Waveform data static or eratic.	Reset. Select chain mode and triangle function.	U12-11, -12, -13, -15 thru -19 and U11-16 thru -19.	All switching with no stuck bits. All lines should be at a different frequency.
Waveform stop address not functional.	Reset. Set stop address to 99.	U11-15	$\overline{\text{LOAD}}$ is a TTL high with a low going pulse every 100 μs. Pulse repetition rate will increase as the stop address is lowered and decrease as the stop address is raised.

Table 6-11. Waveform Memory Troubleshooting (Cont)

Fault	Setup	Check	Results Desired
"Sync Out" not functioning properly.	Reset.	U11-12	SBIT is a TTL high with a low going pulse every 2 ms.
	Select sine function.		Verify that pulse is coincident with end of waveform. Pulse should move through waveform as sync address is adjusted.
"Z-Axis" not functioning properly.	Reset. Press Edit menu key.	U11-11	Verify that ZBIT is low with a high going pulse every 1 ms.
Breakpoints not functioning properly.	Reset.	U11-13	Verify that STBIT is high with a low going pulse every 2 ms.

Table 6-12. Waveform Latch Troubleshooting

Fault	Setup	Check	Results Desired
Waveform data not reaching waveform synthesizer correctly or Control lines (Z-Axis, Sync Out, break-points) not functioning properly.	Reset.	U1-11 U1-2, -5, -6, -9, -12, -15, -16, -19 and U3-2, -5, -6, -9, -12, -15, -16, -19.	Verify the presence of a 1 MHz signal. Verify that the outputs match the inputs (pins 3, 4, 7, 8, 13, 14, 17, 18).
	Adjust waveform editing cursor position.	U24A-5	A high with low going pulses when cursor is adjusted.

Table 6-13. Waveform Synthesizer Troubleshooting

Fault	Setup	Check	Results Desired
No waveform out, amplitude out of tolerance, or offset out of tolerance.	Reset. Select square function.		Verify waveforms and voltages as shown in table 6-14.
Waveform output erratic, not at programmed points.	Reset. Set stop address to 0000. Adjust "Y" value to −2047.	U2-13. U2-14 thru -24. U6-6.	A TTL high. All are low. Approximately −2.5V.
	Slowly adjust "Y" value to +2047.	U6-6	Voltage should smoothly increase to +2.5V.
Sum In not functioning properly.	Reset. Erase current waveform. Apply +5V to "Sum In" connector.	Junction of R34 and F1. U7-6.	Verify +5V. Verify +2.0V.

Table 6-14. Waveform Synthesizer Functional Check

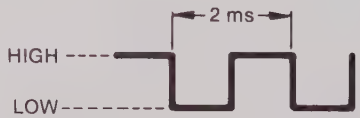
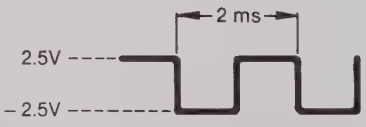
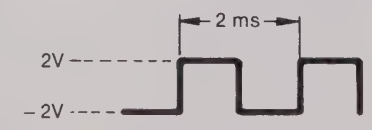
Test Point	Desired Results
U2 pin 4	+10V ±0.1 Vdc
U2 pins 14 thru 24	
U2 pin 13	A high logic level
U6 pin 6	
U7 pin 6	

Table 6-15. Amplitude Control Troubleshooting

NOTE: All logic levels in this circuit are ±5V.

Fault	Setup	Check	Results Desired
No waveform output. Offset out of tolerance.	Reset. Select square function.	U9-3 U9-16 U9-1 U9-4 thru -13 U9-17 U8-6	−5V. +10V. ±2V square wave. Bits represent the binary equivalent of 1000 (1111101000). Pin 4 is most significant. ±1.95V square wave. ±1.95V square wave.
Amplitude control erratic or out of tolerance.	Reset. Set stop address to 0000. Adjust "Y" value to 2047. Set amplitude to 0.500 Vp	U9-1 U9-4 thru -13. U8-6.	−2V Bits represent the binary equivalent of 100 (0001100100). Pin 4 is the most significant. Approximately −195 mV.
	Adjust amplitude to 5.00 V-p.	U9-4 thru -13. U8-6.	No stuck bits. Should smoothly decrease to approximately −1.95V.

Table 6-16. Offset Control Troubleshooting

NOTE: All logic levels in this circuit are ±5V.

Fault	Setup	Check	Results Desired
Offset control erratic or not functional. Offset out of tolerance.	Reset. Set CAL constant to 0, amplitude to 0.1 Vp, and offset to −5.00V.	U5-17 U4-6 U5-4 thru -15	+10V ±0.1 Vdc. −2.5V. Bits represent the binary equivalent of 1048 (010000011000). Pin 4 is most significant.
	Adjust offset from −5V to +5V, setting the amplitude to 1 Vp when offset is between −0.5V and +0.5V	U4-4 thru -14. U4-6.	No stuck bits. Smoothly decreases to −7.5V.

Table 6-17. Output Amplifier Troubleshooting

Fault	Setup	Check	Results Desired
No waveform output. Waveform output distorted or offset.	Reset. Select square function.	U8-6. Junction of R51 and R52.	± 1.95V square wave. ± 10V square wave
	Erase current waveform.	Q7 base Q8 base U10-6 Q7 emitter Q8 emitter Q9 base Q10 base	~ + 13V ~ – 13V ~0V ~ + 13.7V ~ – 13.7V ~ + 0.9V ~ – 0.9V

Table 6-18. Attenuator Troubleshooting

Fault	Setup	Check	Results Desired
No waveform output.	Reset. Select sine function.	K1-14. F2.	20 Vp-p sine wave. 10 Vp-p sine wave on both sides of fuse F2.
Amplitude and offset controls not functioning properly.	Reset. Select sine function. Set amplitude to 5.00 Vp.	R61 (A0) R62 (A1) K1-14 K1-7 K2-7 CR20 anode	+ 5V + 5V 20 Vp-p sine wave. 20 Vp-p sine wave. 20 Vp-p sine wave. 10 Vp-p sine wave.
	Set amplitude to 499.5 mVp.	R61 (A0) R62 (A1) K1-14 K1-7 K2-7 CR20 anode	+ 5V – 5V ~20 Vp-p sine wave. ~20 Vp-p sine wave. 0V. ~1 Vp-p sine wave.
	Set amplitude to 49.95 mVp.	R61 (A0) R62 (A1) K1-14 K1-7 K2-7 CR20 anode	– 5V – 5V ~20 Vp-p sine wave. 0V. 0V. ~.1 Vp-p sine wave.

Table 6-19. Burst Counter Troubleshooting

Fault	Setup	Check	Results Desired
Burst mode not functioning properly. Waveform counter not functioning properly.	Reset. Select burst mode. Set burst count to 1.	U50-3 U50-3 thru -6 U51-3 thru -6 U43-3 thru -6 U40-3 thru -6	A low. All are high. All are high. All are high. All are high.
	Set burst count to 1,048,575.	Burst counter inputs.	All are low. The data on the burst counter inputs should represent the one's complement of the selected burst count.
	Set stop address to 0009.	U50-2 U50-9	1 MHz. A high.
	Press manual trigger key.	U50-7	A low with high going pulse every 10 μs.
	Press manual trigger key repeatedly.	U40-11 thru -14 U43-11 thru -14 U50-11 thru -14 U51-11 thru -14	No stuck bits. No stuck bits. No stuck bits. No stuck bits.
	Press manual trigger key.	U47-11	1 MHz.

Table 6-20. Control Shift Register Troubleshooting

NOTE: Logic levels on U11, U13, U18, and U19 are ±5V.

Fault	Setup	Check	Results Desired
Parameter control not functioning properly. NOTE: If only one parameter. is affected, refer to that circuit's guide for the correct operation of it's control lines.	Reset. Select REF soft key and rotate control knob	U14-2 (SERD)	Low with groups of high going pulses.
		U14-3 (SERC)	Low with groups of high going pulses.
		U14-1 (ANLE)	Low with high going pulses.
		U14-4 (REFSEL)	Switching from high to low.
		U11-4, -14, -15	Same as U14-2, -3, and -1 respectively.

Table 6-21. Z-Axis Driver Troubleshooting

Fault	Setup	Check	Results Desired
Z-Axis Out not functioning properly.	Reset. Press Z-level soft key.	U1-2	A low with high going pulses every 1 ms.
	Set Z-level as shown in table 6-22.	Take measurements as shown in table 6-22.	Values shown in table 6-22.

Table 6-22. Z-Axis Driver Functional Check

Z-level	ZL-2 CR11 Anode	ZL-1 CR12 Anode	ZL-0 CR13 Anode	Q6 Emitter	Q5* Base	Q5* Emitter
2V	Low	Low	Low	−0.6V	2.6 Vdc	2 Vdc
4V	Low	Low	High	−0.6V	4.6 Vdc	4 Vdc
6V	Low	High	Low	−0.6V	6.6 Vdc	6 Vdc
8V	Low	High	High	−0.6V	8.6 Vdc	8 Vdc
10V	High	Low	Low	−0.6V	10.6 Vdc	10 Vdc
12V	High	Low	High	−0.6V	12.6 Vdc	12 Vdc
14V	High	High	Low	−0.6V	14.6 Vdc	14 Vdc

*DC level ± 1V with low going pulses.

Table 6-23. Keyboard Troubleshooting

Fault	Setup	Check	Results Desired
No response from any or all front panel keys.		RN1-1, RN2-1. U32-2, -4, -6, -8, -11, -13, -15, -17. U33-6, -8, -11.	+ 5V. A high. A high.
	Press any key.		Verify appropriate pin on U32 or U33 goes low.
LCD viewing control not functional.	N/A	J12-11	Voltage goes from approximately − 1V to + 2V as viewing angle control is adjusted from full down to full up.

Table 6-24. Control Knob Troubleshooting

Fault	Setup	Check	Results Desired
No response from knob when adjusting all parameters.	Spin Control knob	U34B-5 and U34C-9 Q1 collector	Alternating between high and low and 90° out of phase with each other. A high with low going pulses.

Table 6-25. Liquid Crystal Display Troubleshooting

Fault	Setup	Check	Results Desired
Display blank or totally black. Display characters unintelligible or not updating.	Reset.	J10-3 J10-4, -5, -7, thru -14. J10-6	Voltage swing from approximately − 1V to approximately + 2V as LCD viewing control is adjusted from full down to full up. No stuck bits. Low and then pulses high when any key is pressed.

6.3.2 Microprocessor and Main Memory

Generally, when the instrument is totally nonfunctional, i.e., display is unintelligible, random waveform data or no output, the problem is in the microprocessor section. However, before beginning to troubleshoot this section, check the appropriate dedicated circuits for correct operation. Detailed reading of the circuit description is also very helpful before attempting to find and correct a problem.

Table 6-26. Microprocessor and Main Memory Troubleshooting

Fault	Setup	Check	Results Desired
Nonfunctional operation	N/A	U30-3 (XTAL2)	4 MHz, sinusoid, approximately 0 to 4V.
		U30-21 (VDD)	>4.5 Vdc.
		U30-7 (STBY)	A high
		U30-6 (RESET)	A high
		U30-5 (IRQ)	A high
		U30-4 (NMI)	A high
		U30-40 (E)	1 MHz at 50% duty cycle.
		U30-39 (AS)	1 MHz at approximately 30% duty cycle.
		U30-22 thru -38	No stuck bits.
		U14-2, -5, -6, -9, -12, -15, -16, -19.	No stuck bits.
		U37-7, -9, -12, -14, -16, -18.	No stuck bits.
		U46-2, -5, -6, -9, -12, -15, -16, -19.	No stuck bits.

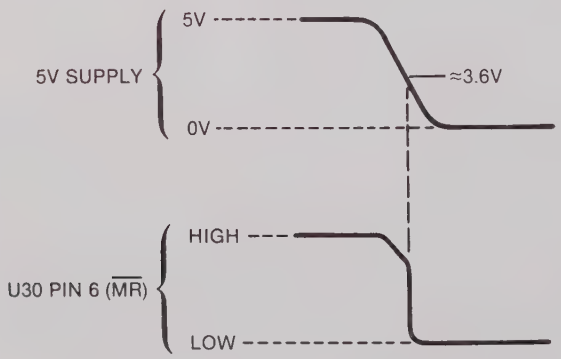


Figure 6-4. Power Off Reset Timing

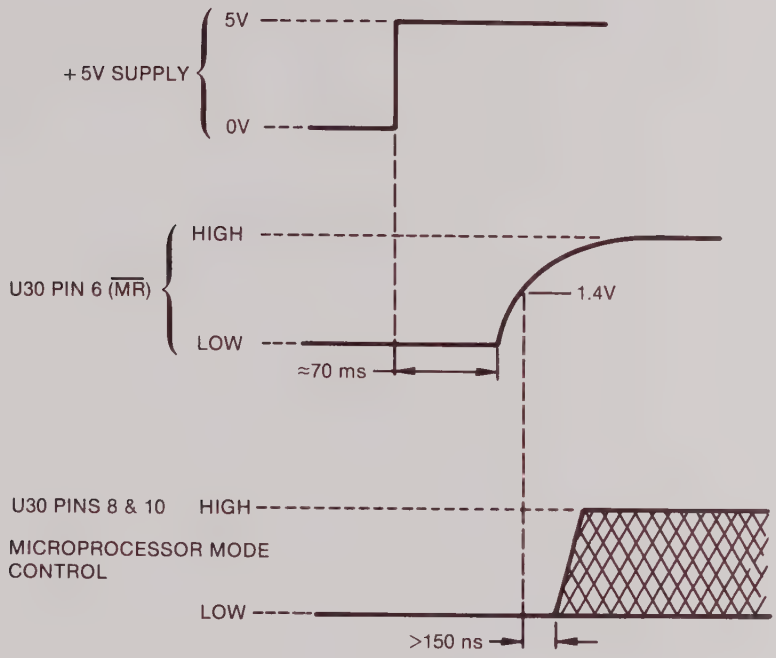


Figure 6-5. Power On Reset Timing

If the address and data busses appear to be functional, the problem may be in the reset and mode setting circuit. The correct reset timing is shown in figure 6-4 and 6-5.

If stored waveforms and instrument settings are not retained when the instrument is powered off, check the battery backup supply. Turn off the instrument and check CR3 cathode (BBV) for > 2 Vdc.

Table 6-27. Communication Option 001 Troubleshooting

Fault	Setup	Check	Results Desired
Non-responsive, in whole or in part.	Cycle power and reset instrument.	U2-3, -5, -7 thru -14, -37, -38, -39. U2-6. U2-4, -16, -17, -18, -21, -22, -23, -25, -26, -27, -29 thru -36, -40.	No stuck bits. 1 MHz. All high.
	Connect instrument to IEEE-488 controller. Set controller in loop that "talks to" and "reads from" the Model 75. As part of loop, generate a programming error (A10I) and then serial poll the unit. NOTE: Figure 6-6 shows a sample program written on a Wavetek Model 6000.	U2-21 and -29. U2-22. U2-40, U3-1 thru -9, -12 thru -19, U4-1 thru -9, -12 thru -17. Logic levels on bus side of U3 and U4.	Both high. A low. No stuck bits. Typically 0 to 3 Vdc.

```
10 DO
20 WRITE @709:"A1OI"
30 READ @709:A
40 STATUS@709:SPOLL
50 LOOP
60 END
```

Figure 6-6. IEEE-488 Sample Check Out Program

Table 6-28. Communication Option 002 Troubleshooting

Fault	Setup	Check	Results Desired
Non-responsive, in whole or in part.	Reset.	U1-6. U1-7. U1-23. U1-9, -11, -13 thru -22.	A 2.4576 MHz sinusoid, approximately 0 to 5V. A high. A low. No stuck bits.
	Set baud rate switches as indicated in table 6-29.	U1-4.	The frequency shown in table 6-29.
	Connect instrument to RS-232-C controller. Set controller in loop that "writes to" and "reads from" the Model 75. NOTE: Figure 6-7 shows a sample program written on a Wavetek Model 6000.	U1-2 and -7, and U3-8. U3-8. U3-3 and -6.	No stuck bits. Logic levels ±12V. Both are +12V.

Table 6-29. Baud Rate Generator Functional Check

Baud Rate	SW1-1	SW1-2	SW1-3	SW1-4	Frequency
19,200	Open	Closed	Closed	Closed	307.2 kHz
9600	Closed	Closed	Closed	Open	153.6 kHz
4800	Open	Closed	Closed	Open	76.8 kHz
2400	Open	Open	Open	Closed	38.4 kHz
1800	Closed	Open	Closed	Open	28.8 kHz
1200	Open	Open	Closed	Open	19.2 kHz
600	Closed	Open	Open	Closed	9.6 kHz
300	Open	Closed	Open	Open	4.8 kHz
200	Open	Closed	Open	Closed	3.2 kHz
150	Closed	Open	Open	Open	2.4 kHz
134.5	Closed	Closed	Open	Closed	2.1 kHz
110	Open	Open	Open	Open	1.7 kHz
75	Open	Open	Closed	Closed	1.2 kHz
50	Closed	Open	Closed	Closed	800 Hz

```
10 DIM A$*60
20 SET @5:HVAL ("8E4F")          !SET UP INTERFACE
30 WRITE @5:"!"                  !GO TO REMOTE
40 DO
50 WRITE @5:"XT3 I?"
60 READ @5:A$
70 LOOP
80 END
```

Figure 6-7. RS-232-C Sample Check Out Program

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than 1 Vdc is measured across its base emitter junction in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage across the base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage or reverse biased, the transistor is defective.
4. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than 1 Vdc (typically 0.7 Vdc) forward voltage across it.

6.4.3 Operational Amplifier

1. Generally the "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 Field Effect Transistor (FET)

No measurable gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective. Gate to source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485 and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

6.4.6 Logic Levels

Table 6-30. Logic Levels by Family (Except Where Otherwise Noted)

Logic Family	Min High	Min Low
74HCxxx	3.15V	0.9V
74HCTxxx*	3.15V	0.9V
74ASxxx	2.0V	0.8V
74LSxxx	2.0V	0.8V
74Fxxx	2.0V	0.8V
4xxx	3.5V	1.5V
Microprocessor and Memories	2.0V	0.8V

*Inputs match 74LSxxx levels and outputs match 74HCxxx levels.

SECTION 7
PARTS LIST AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, is applicable, the function performed.

The number etched into a PC board is the board part number. The assembly (PC board and components on the board) part number is stamped on the board.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0366
Instrument Top Assembly/Parts List	1000-00-0366
Chassis Assembly/Parts List	1101-00-1774
Front Panel Schematic	0103-00-1775
Front Panel Assembly/Parts List	1206-00-1775
Keyboard Assembly/Parts List	1208-00-1376
Rear Panel Assembly/Parts List	1206-00-1776
Microprocessor/ARB Memory Board Schematic	0103-00-1389
Microprocessor/ARB Memory Board Assembly	1100-00-1389
Microprocessor/ARB Memory Board Parts List	1100-00-1389
PPL/Waveform Board Schematic	0103-00-1456
PPL/Waveform Board Assembly	1100-00-1456
PPL/Waveform Board Parts List	1100-00-1456
Rear Panel Assembly/Parts List	1101-00-1771
Power Supply/AC Primary Schematic	0103-00-1113
Power Supply Assembly/Parts List	1208-00-1772
AC Primary Assembly/Parts List	1208-00-1119
GPIB Option Schematic	0103-00-1678
GPIB Option Assembly/Parts List (Sh 2 Only)	1000-00-0426
GPIB Option PCA Assembly/Parts List	1100-00-1678
RS-232-C Option Schematic	0103-00-1677
RS-232-C Option Assembly/Parts List (Sh 2 Only)	1000-00-0427
RS-232-C Option PCA Assembly/Parts List	1100-00-1677

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REV	ECN	BY	DATE	APP
—	RELEASE		7/7/85	
A	6072	JJ	11/21/86	A CT

A1A4 PCA, DISPLAY 1208-00-1874

A1A3 PCA, KEYBOARD 1208-00-1376

A1 ASSY, FRONT PANEL 1206-00-1775

W17 (OPTION 001 ONLY)

P30 J30 — OPTION 001 — W15

COM, COM, COM, COM, COM, COM, REN, DIO8, DIO7, DIO6, DIO5, GND, ATN, SRQ, IFC, NDAC, NRFD, DAV, EOI, DIO4, DIO3, DIO2, DIO1

PCA GPIB OPTION 1100-00-1678

A2A1 ASSY, REAR PANEL 1206-00-1776

P30 J30C J17 W8 W15 — OPTION 002

TXD, RXD, RTS, CTS, DSR, SIG GND, RLSD

RXDATA, TXDATA, —, DTR/CTS, RTS/DSR, SIG GND, RLSDC, —, DTR, DTR/CTS

DCE CONNECTOR

PCA RS232 OPTION 1100-00-1677

P30 J30T W15

TXD, RXD, RTS, CTS, DSR, SIG GND, RLSD

TXDATA, RXDATA, RTS/DSR, CTS/DTR, DSR, SIG GND, RLSDT, DTR, DTR/CTS

DTE CONNECTOR

E4

J27 REF IN (TTL)

J28 REF OUT (TTL)

J24 HOLD IN (TTL)

J25 RETURN IN (TTL)

J26 Z-AXIS OUT (600Ω)

A3 PCA, μPROC / ARB MEM 1100-00-1389

W8 P16 J16: GND, +5V, +15V, -15V, R/W, E, IRQ, MR, AD4, AD5, AD6, AD7, ADRØ, ADR1, ADR2, COMM, ADØ, AD1, AD2, AD3

J6: WBIT1, WBIT2, WBIT3, WBIT4, WBIT5, WBIT6, WBIT7, WBIT8, WBIT9, WBIT10, WBIT11, WBIT12, STBIT, SBIT, ZBIT, GND, EB, GND, CLK, GND

J8: GND, SERD, GND, SERC, GND, PLLE, GND, ANLE, GND, GND, BURLOAD, PCLK, T POINT, SYNC IN, TRIG MASK, STOP DR, FRBIT3, FRBIT2, FRBIT1, NO LOAD

W5 P10 J10 — W6 P12 J12

J11: GND, +5V, DD, ADRØ, R/W, DE, ADØ, AD1, AD2, AD3, AD4, AD5, AD6, AD7

J13: CPRE1, CPRE2, PB9, PB11, PB7, PB6, PB10, PB8, GND, DDH, DD, DDL, PB5, PB4, PB3, PB2, PB1

W2 P7 J7 — W1 P9 J9

P4 J4: RTS, -15V, +5V, +5V, +15V, GND, GND, SLOPE, MANHOLD, GND, GND, STOP, ARB R/W, GND, GND

P5 J5: HOLD IN, RETURN IN, Z-AXIS, RTS, -15V, +5V, STOP, +15V, REF IN, REF OUT, GND, GND, SLOPE, MANHOLD, GND, GND, GND, ARB RAW, GND, GND

A4 PCA, PLL / WAVEFORM 1100-00-1456

BURST TRIG IN (TTL) — DONE OUT (TTL) — SYNC IN (TTL) — SYNC OUT (TTL) — SUM IN (50Ω) — ARB OUT (50Ω)

J18 J19 J20 J21 J22 J23

J31 P31 W9: GND, REF IN, REF OUT, HOLD IN, RETURN IN, Z-AXIS

A2A3 PCA, POWER SUPPLY 1208-00-1772

A2 ASSY, POWER SUPPLY 1101-00-1771

J1 E1 W4 GRN/YEL E2 W3 GRN/YEL E3

A2A2 PCA AC PRIMARY 1208-00-1119

J2 P2: 230V POSITION — 115V POSITION

GRY, WHT/BLK, WHT/GRY, BLK — FROM T1

J3 P3: RED, RED, WHT/RED, BLU, BLU

A2A5 T1 1204-00-0061

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TEPPER	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	7-7-85	TITLE: SCHEMATIC INSTRUMENT
FINISH WAVETEK PROCESS	RELEASE APPR		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75 — DWG NO 0004-00-0366 — REV A
	SCALE		CODE IDENT 23338 — SHEET 1 OF 1

0004-00-0364

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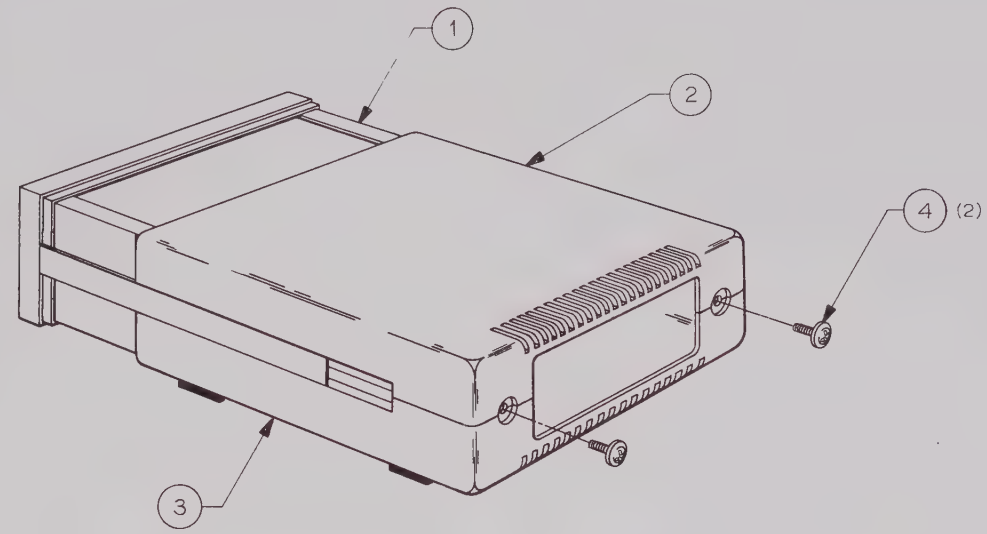
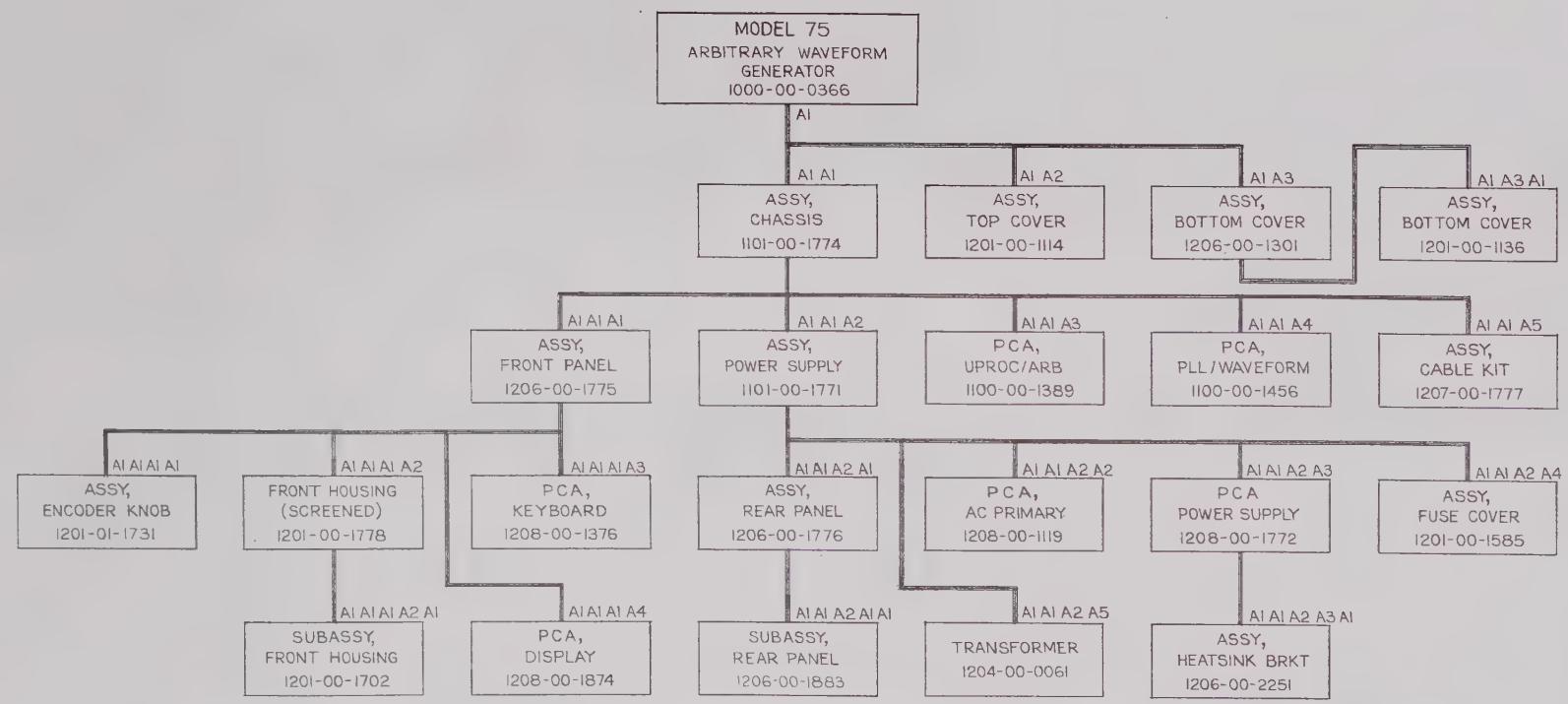
B	6137		3/11/86	R.P.T.





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	OUTLINE DRAWING	0002-00-0366	WVTK	0002-00-0366	1
NONE	SCHEMATIC, INSTRUMENT	0004-00-0366	WVTK	0004-00-0366	1
NONE	CAL PROCEDURE	0006-00-0366	WVTK	0006-00-0366	1
NONE	ACCEPTANCE TEST SPECIFICATIONS	0007-00-0366	WVTK	0007-00-0366	1
1	ASSY, CHASSIS-75	75-1774	WVTK	1101-00-1774	1
2	ASSY, TOP COVER	21-1114	WVTK	1201-00-1114	1
3	ASSY, BOTTOM COVER	1206-00-1301	WVTK	1206-00-1301	1
NONE	INSTRUCTION MANUAL	MANUAL-75	WVTK	1300-00-0366	1
NONE	MODEL 75 QUICK REFERENCE GUIDE	75-0451	WVTK	1300-00-0451	1
4	SCREW, TRUSS HD, CAD I, PHLPS, 10-32X1/2	10-32X1/2 TRS PLPS MS	CMRCL	2800-20-0208	2
NONE	INSERT	101-18	WVTK	3300-00-0015	1
NONE	CARTON	101-18A	WVTK	3300-01-0012	1
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 4/22/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: MODEL 75 ARBITRARY WAVEFORM GENERATOR
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 75 · DWG NO 1000-00-0366 · REV B
	SCALE NONE		SIZE A · CAGE 23338 · SHEET 1 OF 1

1000-00-0366 B

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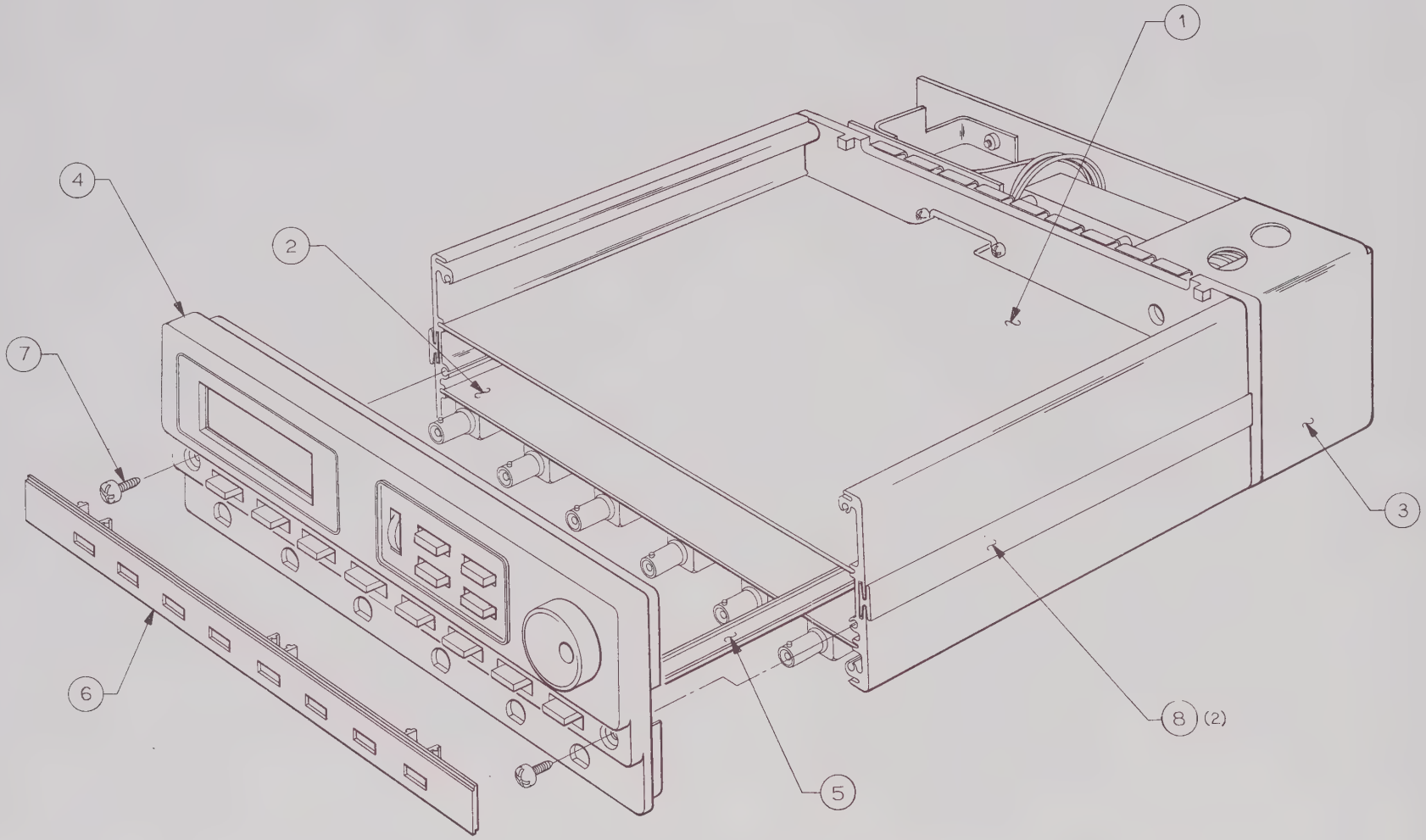

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCA, UPROC/ARB MEM	75-1389	WVTK	1100-00-1389	1
2	ASSY, PLL WAVEFORM BD	75-1456	WVTK	1100-00-1456	1
3	ASSY, POWER SUPPLY-75	75-1771	WVTK	1101-00-1771	1
4	ASSY, FRONT PANEL-75	75-1775	WVTK	1206-00-1775	1
NONE	!ASY! ASSY, CABLE KIT-75	75-1777	WVTK	1207-00-1777	1
5	POWER ROD	21-6201	WVTK	1400-01-6201	1
8	INSERT, SIDE PANEL	20-7910	WVTK	1400-01-7910	2
6	BEZEL, KEY-75	75-8710	WVTK	1400-01-8710	1
7	SCREW, SELF TAPPING TYPE B, PAN CROSS	8-18 X 1/2	CMRCL	2800-22-8208	2

2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. SEE 0004-00-0366 FOR INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL —//—
FINISH WAVETEK PROCESS —//—

DRAWN A. TALMADGE DATE 5/14/85
PROJ ENGR M. S. Muth 7/2/85
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO • CALIFORNIA
TITLE ASSEMBLY, CHASSIS
MODEL NO. 7[illegible]
DWG NO. 1101-00-1774
REV. A
CODE IDENT 23338
SHEET 1 OF 1

1101-00-1774 A

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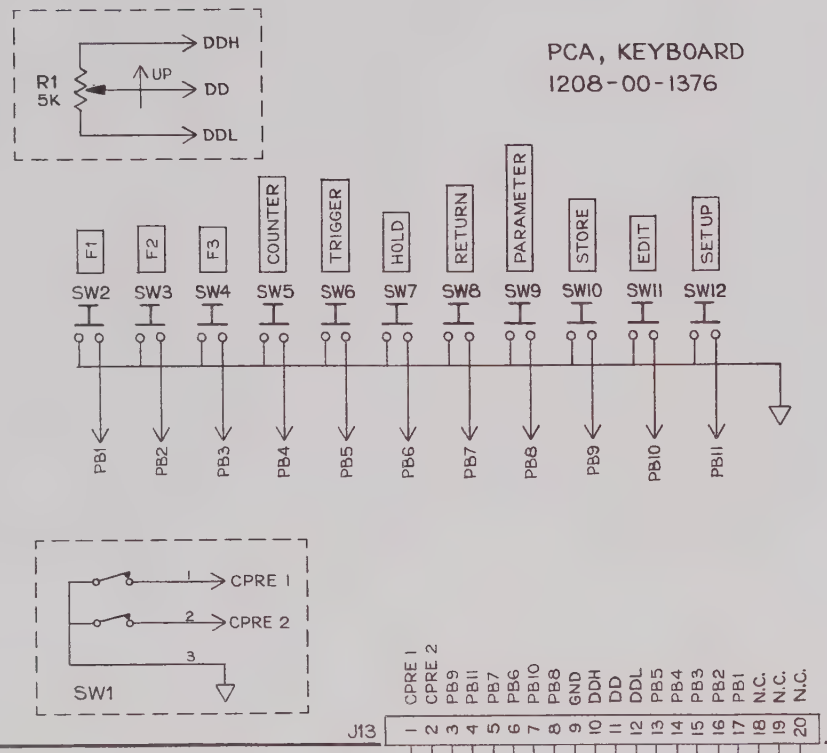
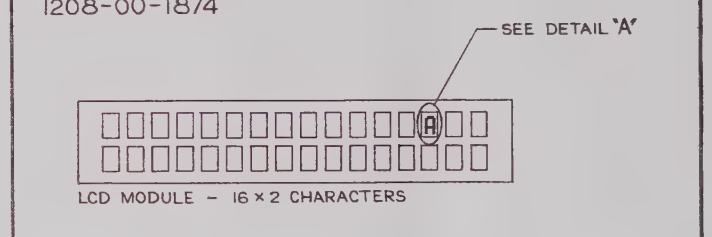
REV	ECN	BY	DATE	APP

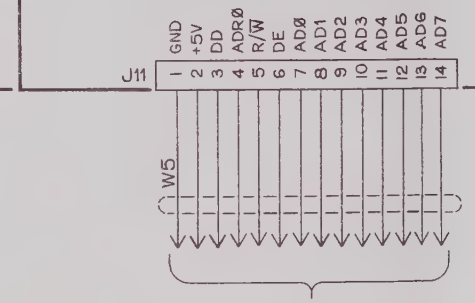
PCA, KEYBOARD
1208-00-1376

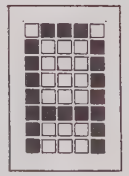


ASSEMBLY, FRONT PANEL
1206-00-1775

PCA, DISPLAY
1208-00-1874







DETAIL "A"

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 2/21/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE: SCHEMATIC, FRONT PANEL
FINISH WAVETEK PROCESS —	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 15 / DWG NO 0103-00-1775 / REV —
	SCALE —		CODE IDENT 23338 / SHEET 1 OF 1

0103-00-1775 —

BISHOP GRAPHICS-ACCUPRESS REORDER NO. A27888

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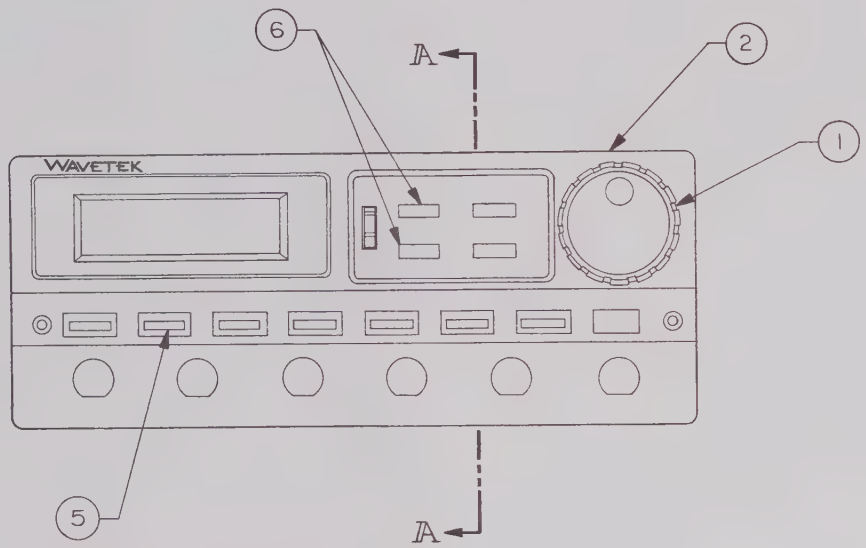
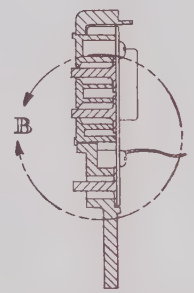
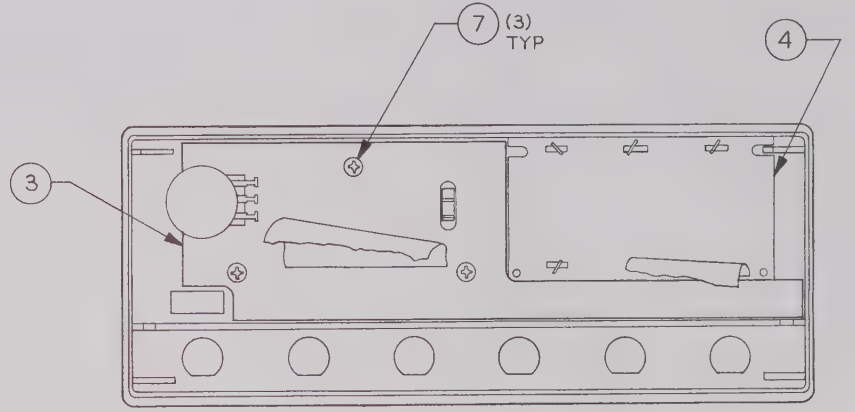
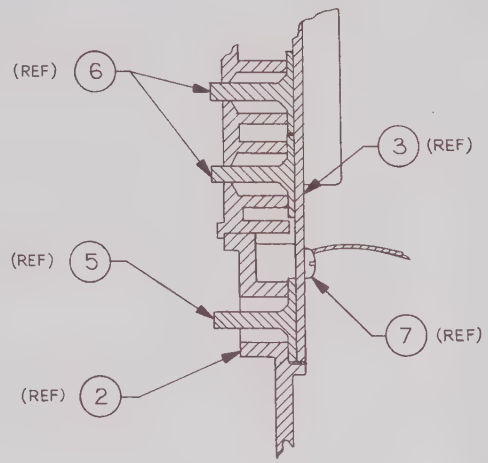
REV	ECN	BY	DATE	APP





SECTION A





DETAIL B
SCALE: 2/1

REFERENCE DESIGNATORS	PART DESCRIPTION	DRIO-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, FRONT PANEL	0103-00-1775	WVTK	0103-00-1775	1
1	ASSY, ENCODER KNOB	23-1731	WVTK	1201-00-1731	1
2	ASSY, FRONT HOUSING, SCREENED	75-1778	WVTK	1201-00-1778	1
3	PCA, KEYBOARD	23-1376	WVTK	1208-00-1376	1
4	PCA, DISPLAY BD	23-1874	WVTK	1208-00-1874	1
5	KEY PAD STRIP	21-6230	WVTK	1400-01-6230	1
6	KEYPAD STRIP MOD MF: 1400-01-6230	1400-01-9409	WVTK	1400-01-9409	2
7	SCREW, SELF TAPPING TYPE B, PAN CROSS RECESS, 4-24X1/4	4-24 X 1/4	CMRCL	2800-22-4142	3

1206-00-1775 —

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN AMY TALMADGE 1/7/04
PROJ ENGR 7/24/05
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030
DO NOT SCALE DWG
SCALE FULL & AS NOTED

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY, FRONT PANEL - 75

MODEL NO 75
DWG NO 1206-00-1775
REV —
CODE IDENT 23338
SHEET 1 OF 1

1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0366

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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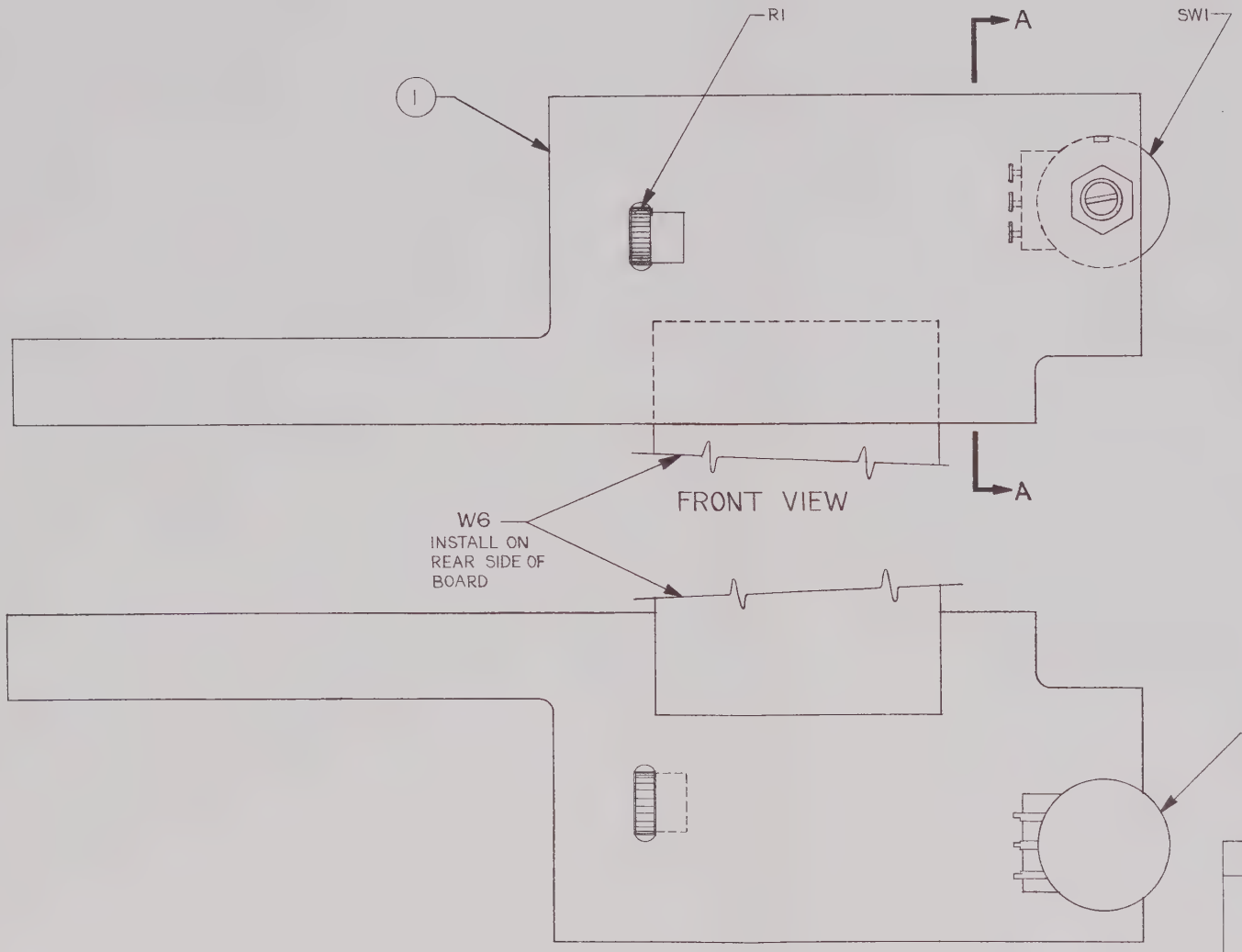
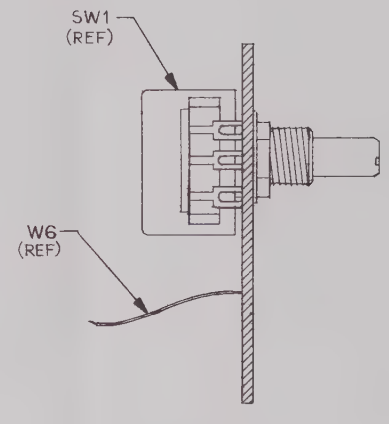
REV	ECN	BY	DATE	APP





SECTION A-A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	PCB KEYBOARD	1700-00-1376	WVTK	1700-00-1376	1
R1	POT, 5K	4600-05-0211	WVTK	4600-05-0211	1
SW1	SWITCH, ROTARY ENCODER	5104-00-0026	WVTK	5104-00-0026	1
W6	CABLE, FLEX FLAT 2IN 20 PIN	1-88665-9	AMP	6001-60-0008	1

1 SEE 0103-00-1701 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 12/13/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR M.S. Muth	6/26/85	TITLE PCA, KEYBOARD BOARD
	RELEASE APPROV D.P. Fish	6/26/85	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 23/75	DWG NO 1208-00-1376 REV A
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 1

1208-00-1376 A

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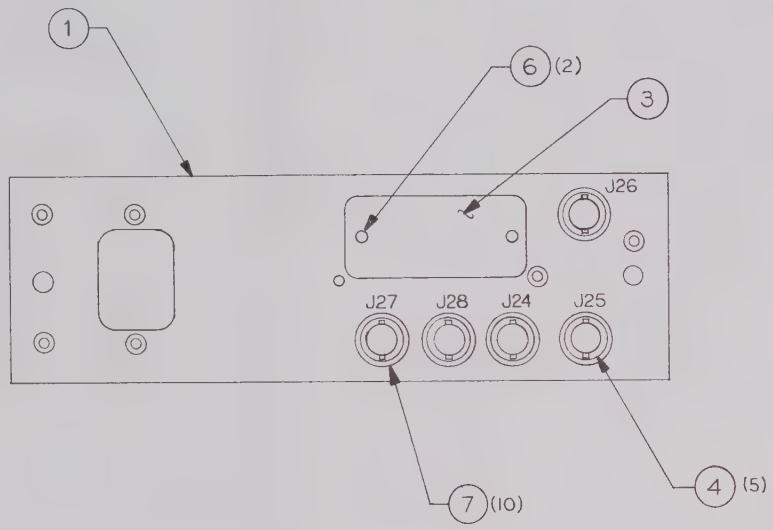
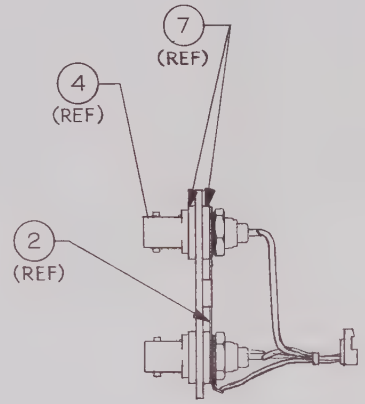
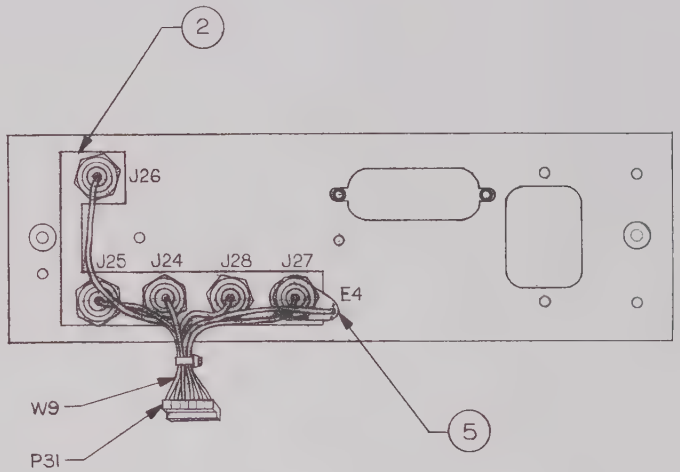
REV	ECN	BY	DATE	APP







SIGNAL	FROM	TO	COLOR
GROUND	E4	P31, PIN 1	WHT/BRN
REF IN	J27	P31, PIN 2	WHT/RED
REF OUT	J28	P31, PIN 3	WHT/ORN
HOLD	J24	P31, PIN 4	WHT/YEL
RETURN	J25	P31, PIN 5	WHT/GRN
Z AXIS	J26	P31, PIN 6	WHT/BLU

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	SUB ASSY, REAR PANEL	75-1883	WVTK	1206-00-1883	1
2	STRAP, BNC GROUND	75-8745	WVTK	1400-01-8745	1
3	COVER PLATE	23/75-9653	WVTK	1400-01-9653	1
4	BNC CONN	KC-7946	KINQ	2100-01-0002	5
5	SOLDER LUG	1497	SMITH	2100-04-0012	1
6	RIVET, SNAP, PLASTIC	SR-4050	RICH	2800-12-0046	2
7	WASHER, SHOULDER	2668	SMITH	2800-27-0004	10

2. WIRES & CABLES OBTAINED FROM CABLE KIT 1207-00-1777.
1. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0366.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN A.TALMADGE DATE 1/25/85
PROJ ENGR M.S. Mullen 2/4/85
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE FULL

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
ASSEMBLY, REAR PANEL

MODEL NO	DWG NO	REV
75	1206-00-1776	—
CODE IDENT 23338	SHEET 1 OF 1	

1206-00-1776 —

BISHOP GRAPHICS/ACCUPRESS REORDER NO A27086

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REV	ECN	BY	DATE	APP
C	RELEASED			
D	6072, 6083			
E	7256			PRT

J6 — TO PLL/WAVEFORM BD

(3A5) WBIT1	1
(3A5) WBIT2	2
(3A5) WBIT3	3
(3A5) WBIT4	4
(3A5) WBIT5	5
(3A5) WBIT6	6
(3A5) WBIT7	7
(3A5) WBIT8	8
(3B5) WBIT9	9
(3B5) WBIT10	10
(3B5) WBIT11	11
(3B5) WBIT12	12
(3B5) STBIT	13
(3B5) SBIT	14
(3B5) ZBIT	15
GND	16
(3A8) $\overline{EB}$	17
GND	18
(3D6) CLK	19
GND	20

J8 — TO PLL/WAVEFORM BD

GND	1
(2B8) SERD	2
GND	3
(2B8) SERC	4
GND	5
(2B7) PLLE	6
GND	7
(2B7) ANLE	8
GND	9
GND	10
(3A8) BURLOAD	11
(2B1) PCLK	12
(3A6) TPOINT	13
(3D8) $\overline{SYNC\ IN}$	14
(J14-19) $\overline{TRIGMASK}$	15
(3D6) $\overline{STOPOK}$	16
(2B7) FRBIT3	17
(2B7) FRBIT2	18
(2B7) FRBIT1	19
(3D8) NO LOAD	20

J10 — TO DISPLAY

GND	1
+5	2
(J12-11) DD	3
(2C5) ADR0	4
(2D6) R/$\overline{W}$	5
(3B1) DE	6
(2C6) AD0	7
(2C6) AD1	8
(2C6) AD2	9
(2C6) AD3	10
(2C6) AD4	11
(2C6) AD5	12
(2C6) AD6	13
(2C6) AD7	14

J12 — TO KEYBOARD

(3C1) CPRE1	1
(3C1) CPRE2	2
(3C1) PB9	3
(3C1) PB11	4
(3C1) PB7	5
(3C1) PB6	6
(3C1) PB10	7
(3C1) PB8	8
GND	9
(3B3) DDH	10
(J10-3) DD	11
(3B3) DDL	12
(3C1) PB5	13
(3C1) PB4	14
(3C1) PB3	15
(3C1) PB2	16
(3C1) PB1	17
	18
	19
	20

J14 — TO BREAKAWAY BD

+5	1
+5	2
GND	3
GND	4
(2B2) BC1	5
(2B2) BC2	6
(2B2) BC3	7
(2D1) AD0	8
(2D1) AD1	9
(2D1) AD2	10
(2D1) AD3	11
(2D1) AD4	12
(2C1) AD5	13
(2C1) AD6	14
(2C1) AD7	15
(J6-19) CLK	16
(3D6) BCEN	17
(3D7) STOPOK	18
(J8-15) $\overline{TRIGMASK}$	19
(P4B-4) $\overline{MANHOLD}$	20
(P4B-3) SLOPE	21
	22
(2A2) LDB0	23
(2A2) LDB1	24
(2A2) LDB2	25
(2A2) LDB3	26
(2A2) LDB4	27
(2A2) LDB5	28
(2A2) LDB6	29
(2A2) LDB7	30
(2D6) E	31
(3A7) $\overline{BURLOAD}$	32
(2A2) OUT2EN	33
(2A2) OUT3EN	34
(2A2) OUT4EN	35

J16 — TO COMM BOARD

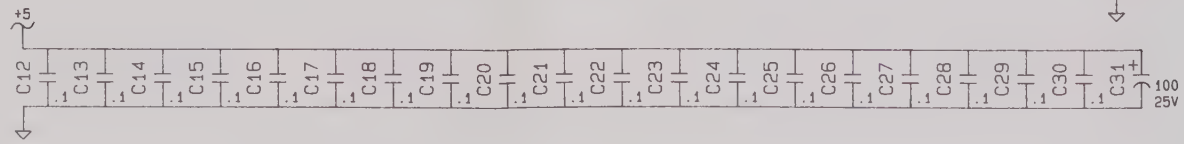
GND	1
+5	2
+15	3
-15	4
(2D6) R/$\overline{W}$	5
(2D6) E	6
(2B5) IRQ	7
(2C7) $\overline{MR}$	8
(2C6) AD4	9
(2C6) AD5	10
(2C6) AD6	11
(2C6) AD7	12
(2C5) ADR0	13
(2C5) ADR1	14
(2C5) ADR2	15
(2B3) $\overline{COMM}$	16
(2C6) AD0	17
(2C6) AD1	18
(2C6) AD2	19
(2C6) AD3	20

P4 — FROM POWER SUPPLY

	A1	GND	B1
	A2	GND	B2
	A3	(J14-21) SLOPE	B3
(3C1) $\overline{RTS}$	A4	(J14-20) $\overline{MANHOLD}$	B4
-15	A5	GND	B5
+5	A6	GND	B6
+5	A7	(3A7) $\overline{STOP}$	B7
+15	A8	(3A7) ARB R/W	B8
	A9	GND	B9
	A10	GND	B10

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBERS +5	PIN NUMBERS GND
U1		7
U2	14	7
U3	14	7
U4	14	7
U5	14	7
U6	14	7
U7		7
U8	14	7
U9	16	8
U10	14	7
U13	16	8
U14	20	10
U15	14	7
U16	20	10
U17	20	10
U18	16	8
U19	16	8
U22	20	10
U23	16	8
U24	16	8
U25	16	8
U26	20	10
U27	16	8
U28	16	8
U29	16	8
U32	20	10
U33	20	10
U34	14	7
U35	14	7
U36	16	8
U37	20	10
U38	14	7
U39	20	10
U40	16	8
U41	16	8
U42	20	10
U43	16	8
U44	20	10
U45	20	10
U46	20	10
U47	20	10
U48	14	7
U49	20	10
U50	16	8
U51	16	8



5. RAM MAY BE EITHER HM6116LP-4 OR HM6264LP-15 OR THEIR EQUIVELENTS. SEE PARTS LIST. FOR 6116 TYPE INSTALL JUMPER E1 TO E3. FOR 6264 TYPE INSTALL JUMPER E1 TO E2.
4. CAPACITORS VALUED IN MICROFARADS (uF).
3. RESISTORS VALUED IN OHMS, 1/8W.
2. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0366.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A3.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TARR	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR S. GREGORY		TITLE SCHEMATIC, uPROC/ARB BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 75 · DWG NO 0103-00-1389 · REV E
	SCALE		CODE IDENT 23338 · SHEET 1 OF 4

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REV	ECN	BY	DATE	APP

POWER ON/OFF RESET

MICROPROCESSOR

MAIN MEMORY

ADDRESS DECODER

BATTERY AND TEST

START ADDRESS PRELOAD

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, uPROC/ARB BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75 · DWG NO 0103-00-1389 · REV E
	SCALE		CODE IDENT 23338 · SHEET 2 OF 4

BISHOP GRAPHICS ACCUPRESS REORDER NO. A2786

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REV	ECN	BY	DATE	APP

WAVEFORM ADDRESS COUNTER

U10C HCT10 · U35C HC10 · U4C AS00 · U15C HC02 · R24 2.49K · U8E HC04

U24 · U25 · U28 · U36 — HC161 (CLR, LOAD, ENT, ENP, CLK, RCO, A, B, C, D, QA, QB, QC, QD)

WAVEFORM ADDRESS SELECTOR

U5B 1/2 F74 · U5A 1/2 F74 (SET, CLK, D, CLR, Q, $\overline{Q}$)

U10A HCT10 · U6A AS08 · U4A AS00 · U3D HC00 · U15A HC02 · U15B HC02 · U3C HC00 · U2C HC04 · U8A HC04 · U8B HC04 · U8D HC04 · U15D HC02

U29 · U19 · U18 · U23 — HC157 (A/$\overline{B}$, EN, 1A–4A, 1B–4B, 1Y–4Y)

WAVEFORM MEMORY

U16 · U17 — HC245 (EN, DIR [BA], DIR [AB], A1–A8, B1–B8)

U7A · U7B — 4066

U11 · U12 — 6264LP-15 (VCC, CS1, CS2, OE, WE, I/O1–I/O8, A0–A12, GND)

C10 .1

R25 49.9K · R26 49.9K

FRONT PANEL INTERFACE

U32 · U33 — HC244 (BE, AE, Y1–Y8, A1–A8)

RN1 · RN2 470K

R27 221K · R28 221K · R29 3.57K · R30 15K · R31 3.32K

U34B HC86 · U34C HC86 · U35B HC10 · U35A HC10 · U8C HC04 · U2B HC04 · U6B AS08 · U10B HCT10 · U2E HC04 · Q1 2N3904

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, uPROC/ARB BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		MODEL NO 75 · DWG NO 0103-00-1389 · REV E
	DO NOT SCALE DWG		CODE IDENT 23338 · SHEET 3 OF 4
	SCALE		

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS-ACCUPRESS REORDER NO. A27888

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REV	ECN	BY	DATE	APP

BREAKAWAY BOARD

DATA LATCH

BURST COUNTER PRELOAD

BURST COUNTER

U46 HC373 — J15-31 E; AD0–AD7

U49 HC374 — J15-35 OUT4EN; J15-32 BURLOAD; J15-17 BCEN

U50 HC161 — RCO, STOPOK → J15-18

U51 HC161

U43 HC161

U41 HC161

U40 HC161 — SLOPE → J15-21; MANHOLD → J15-20; TRIGMASK → J15-19

U47 HC374 — J15-5 BC1

U42 HC374 — J15-6 BC2

U44 HC374 — J15-7 BC3

U45 HC374 — J15-34 OUT3EN

U39 HC374 — J15-33 OUT2EN; J15-23 LDB0 … J15-30 LDB7

J15-8 AD0 … J15-15 AD7

U38A HC10 — J15-5 BC1, J15-6 BC2, J15-7 BC3

U48D HC00 — J15-16 CLK

U48A HC00

U48B HC00

U38B HC10

U38C HC10

U48C HC00

C32 100 25V; C33–C39 .1

J15
TO MAIN BOARD

	+5	1
	+5	2
	GND	3
	GND	4
(A7, D3)	BC1	5
(A7, C3)	BC2	6
(A7, B3)	BC3	7
(C8)	AD0	8
(C8)	AD1	9
(C8)	AD2	10
(C8)	AD3	11
(C8)	AD4	12
(C8)	AD5	13
(C8)	AD6	14
(B8)	AD7	15
(A6)	CLK	16
(D5)	BCEN	17
(B4)	STOPOK	18
(B4)	TRIGMASK	19
(B4)	MANHOLD	20
(B4)	SLOPE	21
	NO CONNECT	22
(B5)	LDB0	23
(B6)	LDB1	24
(B6)	LDB2	25
(B6)	LDB3	26
(B6)	LDB4	27
(B6)	LDB5	28
(B6)	LDB6	29
(B6)	LDB7	30
(D7)	E	31
(D5)	BURLOAD	32
(B6)	OUT2EN	33
(C6)	OUT3EN	34
(D6)	OUT4EN	35

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN
PROJENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.020
DO NOT SCALE DWG
SCALE
DATE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC, uPROC/ARB BOARD

MODEL NO. 75 | DWG NO. 0103-00-1389 | REV E

CODE IDENT 23338 | SHEET 4 OF 4

BISHOP GRAPHICS/ACCUPRESS PREORDER NO. A27099

REV	ECN	BY	DATE	APP
C	FOR RELEASE		7/29/85	
D	7486		5/6/86	A.P.I

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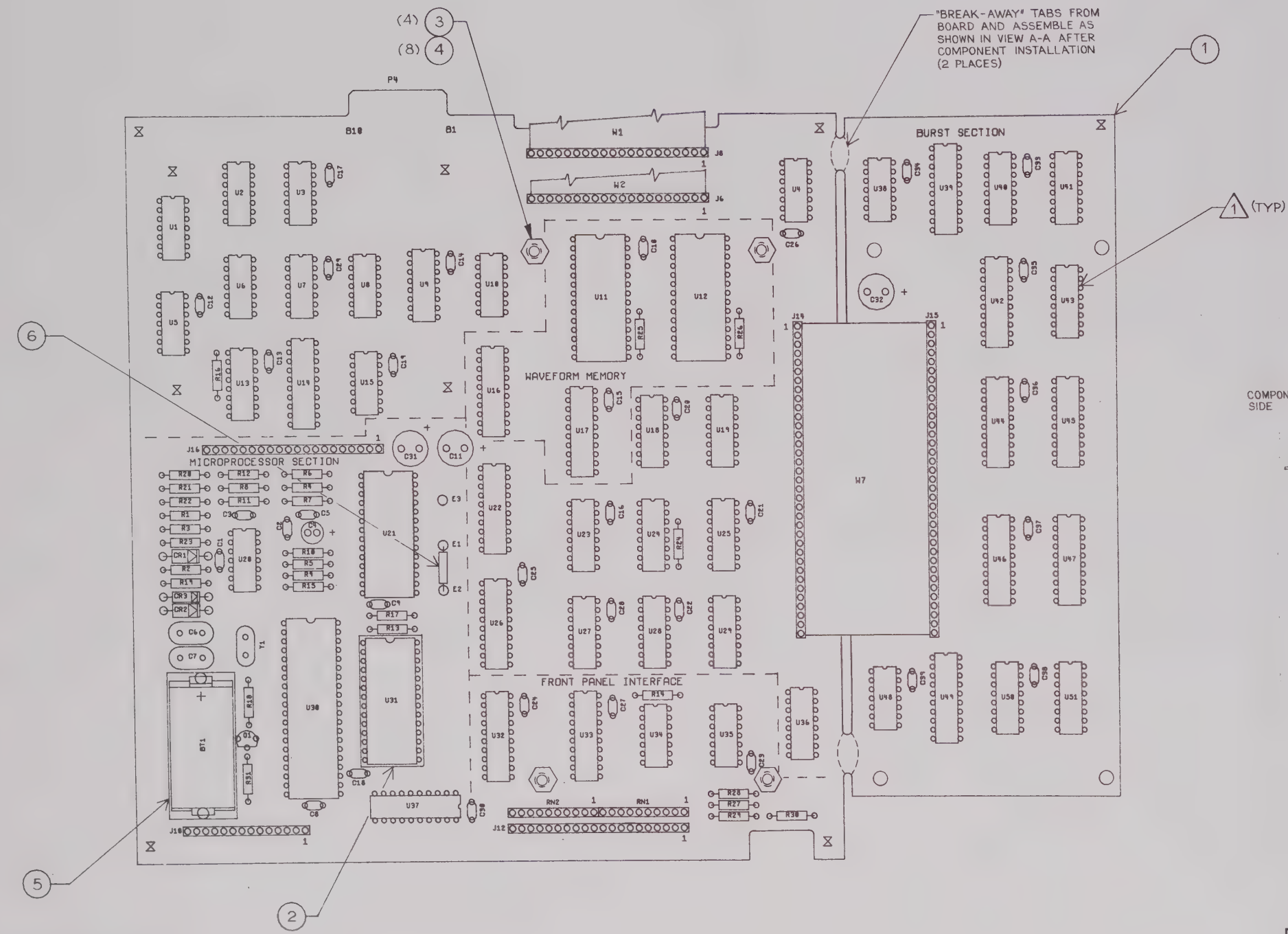

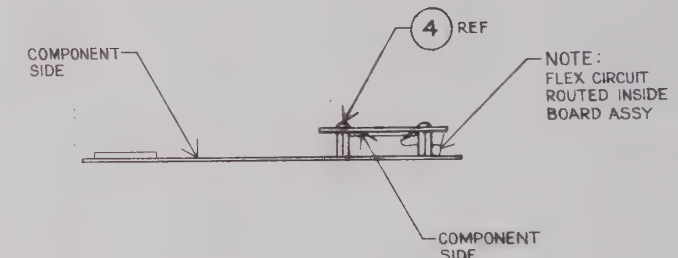

VIEW A-A
(SCALE: NONE)

3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0366.

2. SEE 0103-00-1839 FOR SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1 A1 A3.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-1389

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 3-15-85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE PCA, UPROC-ARB
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 75	DWG NO. 1100-00-1389 REV D
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

1100-00-1389 D

REV	ECN	BY	DATE	APP

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA, UPROC ARB MEM	0103-00-1389	WVTK	0103-00-1389	1
C1 C10 C12 C13 C14 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C33 C34 C35 C36 C37 C38 C39 C5 C8 C9	CAP, CER, MN, .1MF, 50V, Z5U, +80/-20% RAD LD SP .2	5028ES50RD104Z	KYCRA	1500-01-0420	33
C6 C7	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C11 C31 C32	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	3
C4	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	1
1	UPROC/ARB MEM BD	1700-00-1389	WVTK	1700-00-1389	1
J12 J16	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0151	2
J10	HEADER CONNECTOR, 14 PIN	643114-1	AMP	2100-02-0161	1
2	SOCKET, IC, 28 PIN	DILB28P-108T	BURND	2100-03-0081	1
Y1	CRYSTAL, 4MHZ	180-502	WVTK	2300-99-0004	1
3	STANDOFF .625H, .250 HEX, 4-40	8835	SMITH	2800-02-0033	4
4	SCREW, SELF LOCKING, PAN CROSS RECESS	4-40 X 1/4	CMRCL	2800-23-4104	8

WAVETEK PARTS LIST | TITLE: PCA, UPROC/ARB MEM | ASSEMBLY NO. 1100-00-1389 | REV D | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
5	BATTERY HOLDER	BH 2/3A	MPD	3000-00-0137	1
BT1	BATTERY, 3V LITHIUM	BR-2/3A	PANAS	4000-02-0008	1
R11 R8 R9	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	3
R15 R3 R7	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	3
R13 R14 R2 R5	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R1	RES, MF, 1/8W, 1%, 11.8K	RN55D-1182F	TRW	4701-03-1182	1
R20	RES, MF, 1/8W, 1%, 14.3K	RN55D-1432F	TRW	4701-03-1432	1
R6	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
R30	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	1
R19	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	1
R23	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	1
R27 R28 R4	RES, MF, 1/8W, 1%, 221K	RN55D-2213F	TRW	4701-03-2213	3
R21	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R24	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R12	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R18	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1

WAVETEK PARTS LIST | TITLE: PCA, UPROC/ARB MEM | ASSEMBLY NO. 1100-00-1389 | REV D | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R22	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R31	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R29	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R10 R17 R25 R26	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	4
RN1 RN2	RES MODULE, 470K	810-1-474-J	TRW	4770-00-0034	2
6	RESISTOR, 0 OHM JUMPER	JP02T68Q	ROHM	4799-00-0087	1
CR1	DIODE	1N746A	FAIR	4801-01-0746	1
CR2	DIODE	MBR 120	MOT	4806-02-0120	1
CR3	DIODE	5082-2811	HP	4809-02-2811	1
Q1	TRANS	2N3904	FAIR	4901-03-9040	1
W7	CABLE, FLEX, FLAT, 2IN. 35 PIN	3-88665-4	AMP	6001-60-0009	1
W1	CABLE, FLEX, FLAT	1-86943-9	AMP	6001-60-0012	1
W2	CABLE, FLAT, FLEX	1-88684-9	AMP	6001-60-0013	1
U20	IC	MLM339P	MOT	7000-03-3900	1
U11 U12 U21	IC, 64K STATIC RAM	HM6264LP-15	HTACH	8000-62-6400	3
U30	IC, CMOS 8 BIT MCU	HD6303R	HTACH	8000-63-0300	1

WAVETEK PARTS LIST | TITLE: PCA, UPROC/ARB MEM | ASSEMBLY NO. 1100-00-1389 | REV D | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U4	IC, QUAD, 2-INPUT POS-NAND GATES	SN74AS00	TI	8000-74-0020	1
U3 U48	IC, QUAD 2-INPUT NAND	8000-74-0011	WVTK	8000-74-0040	2
U15	IC, QUAD 2-INPUT NOR GATE	MM74HC02	NSC	8000-74-0240	1
U2 U8	IC, HEX INVERTER	MM74HC04	NSC	8000-74-0440	2
U6	IC, QUAD 2-INPUT POS-NAND GATES	SN74AS08	TI	8000-74-0820	1
U35 U38	IC, 3 INPUT NAND	74HC10	MOT	8000-74-1040	2
U10	IC, TRIPLE 3-INPUT NAND GATE	CD74HCT10	RCA	8000-74-1041	1
U5	IC, DUAL D-TYPE FLIP-FLOP	74F74	FAIR	8000-74-7402	1
U1 U7	IC, QUAD BILATERAL SWITCH	CD4066BE	RCA	8001-40-6600	2
U13 U27 U9	IC, 1 OF 8 DECODER/ DEMULTIPLEXER	8007-41-3811	WVTK	8007-41-3840	3
U18 U19 U23 U29	IC, 2 INPUT MUX	74HC157	MOT	8007-41-5740	4
U24 U25 U28 U36 U40 U41 U43 U50 U51	IC, PROGRAMMABLE COUNTER	74HC161	MOT	8007-41-6140	9

WAVETEK PARTS LIST | TITLE: PCA, UPROC/ARB MEM | ASSEMBLY NO. 1100-00-1389 | REV D | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U32 U33 U37	IC, OCTAL TRI-STATE BUFFER	MM74HC244	NSC	8007-42-4440	3
U16 U17	IC, OCTAL TRI-STATE TRANSCEIVER	MM74HC245	NSC	8007-42-4540	2
U14 U46	IC, OCTAL D-TYPE TRANSPARENT LATCH	74HC373	MOT	8007-43-7340	2
U22 U26 U39 U42 U44 U45 U47 U49	OCTAL D-FLIP FLOP, HCMOS, TRISTATE 20 PIN DIP	74HC374	TI	8007-43-7440	8
U34	IC, QUAD 2-INPUT EXCLUSIVE OR	74HC86	MOT	8007-74-8640	1
U31	IC, PROGRAMMED REF: 8002-72-5600	8600-00-0315	WVTK	8600-00-0315	1

WAVETEK PARTS LIST | TITLE: PCA, UPROC/ARB MEM | ASSEMBLY NO. 1100-00-1389 | REV D | PAGE 5

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST UPROC/ARB MEM
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75 / DWG NO 1100-00-1389 / REV D
	SCALE		CODE IDENT 23338 / SHEET OF

BISHOP GRAPHICS-ACCUPRESS REORDER NO. A27088

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REV	ECN	BY	DATE	APP
B	RELEASED			
C	6072, 6083			
D	7256			R.C.T

J7
TO uPROC/ARB BD

(3B7) WBIT1	1
(3B5) WBIT2	2
(3B5) WBIT3	3
(3B5) WBIT4	4
(3B5) WBIT5	5
(3B5) WBIT6	6
(3B5) WBIT7	7
(3B5) WBIT8	8
(3B7) WBIT9	9
(3B5) WBIT10	10
(3B7) WBIT11	11
(3B7) WBIT12	12
(3B7) STBIT	13
(3B7) SBIT	14
(3B7) ZBIT	15
GND	16
(3C7) $\overline{EB}$	17
GND	18
(3B6) CLK	19
GND	20

J9
TO uPROC/ARB BD

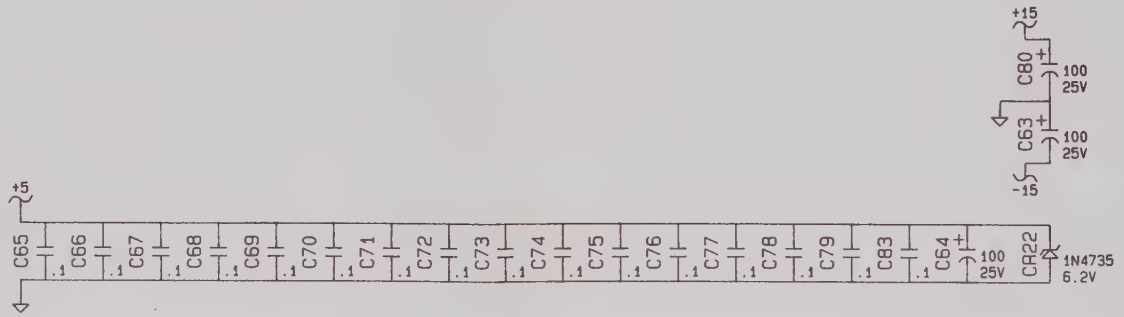
GND	1
(2D8) SERD	2
GND	3
(2D8) SERC	4
GND	5
(2D8) PLLE	6
GND	7
(2B8) ANLE	8
GND	9
	10
(3D4) BURLOAD	11
(3B2) PCLK	12
(3C5) TPOINT	13
(3D1) $\overline{SYNC\ IN}$	14
(3D5) $\overline{TRIGMASK}$	15
(3C6) $\overline{STOPOK}$	16
(2C2) FABIT3	17
(2C2) FABIT2	18
(2C2) FABIT1	19
(3C7) NO LOAD	20

P5
FROM POWER SUPPLY

(3D2) HOLD IN	A1	GND	B1
(3C2) RETURN IN	A2	GND	B2
(3A4) Z-AXIS	A3	(3D7) SLOPE	B3
(3C1) $\overline{RTS}$	A4	(3C4) $\overline{MANHOLD}$	B4
-15	A5	GND	B5
+5	A6	GND	B6
(3B6) $\overline{STOP}$	A7	GND	B7
+15	A8	(3C8) ARB R/W	B8
(3B5) REF IN	A9	GND	B9
(3B2) REF OUT	A10	GND	B10

POWER & GROUND TABLE

REFERENCE DES.	PIN NUMBERS +5	PIN NUMBERS ⏚
U1	20	10
U3	20	10
U12	14	7
U15	14	7
U16	14	7
U20	14	7
U21	14	7
U22	14	7
U23	14	7
U24	14	7
U25	14	7
U26	14	7
U27	14	7
U28	16	8
U29	16	8
U32	14	7
U33	16	8
U34	16	8
U35	16	8
U37	16	8



10. ALL DIODES ARE 1N4148.
9. TRANSISTORS HAVE HEAT SINK (2800-11-0001) AND TRANSIPAD (2800-11-0017).
8. INDICATES GROUND REFERENCED DIRECTLY TO OUTPUT.
7. INDICATES REFERENCE GROUND.
6. INDICATES ANALOG GROUND.
5. ⏚ INDICATES DIGITAL GROUND.
4. CAPACITORS VALUED IN MICROFARADS (uF).
3. RESISTORS VALUED IN OHMS, 1/8W.
2. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0366
1. PARTIAL REFERENCE DESIGNATIONS SHOWN PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A4.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN A.TARR DATE
PROJENG S.GREGORY
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE SCHEMATIC, PLL/WAVEFORM BOARD

MODEL NO. 75 | DWG NO. 0103-00-1456 | REV D

CODE IDENT 23338 | SHEET _ OF _

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REV	ECN	BY	DATE	APP

FREQUENCY SYNTHESIZER

U36 MC145155
J9-4 (BB) SERC
J9-2 (BB) SERD
J9-6 PLLE
6.144MHz
U30A CA082
U30B CA082
U31 VCO LS624
U32A 1/2 HC107
U32B 1/2 HC107
U37 HC151
U35B 1/2 HC390
U34B 1/2 HC390
U35A 1/2 HC390
U34A 1/2 HC390
U33B 1/2 HC390
U33A 1/2 HC390
U28A 1/2 HC390
U29 HC151
J9-17 FRBIT3
J9-18 FRBIT2
J9-19 FRBIT1

CONTROL SHIFT REGISTER

U14 4094
J9-8 ANLE
J9-2 (DB) SERD
J9-4 (DB) SERC
REFSEL (3B4)
ZL0 (3A6)
ZL1 (3A7)
ZL2 (3A8)
BURST (3C7)
TGL (3D7)
CONT (3D6)
GATE (3C7)
U11 4053
U13 4094
OFF12 (4B7)
OFF11 (4B7)
OFF10 (4B7)
OFF9 (4B7)
OFF8 (4B7)
OFF7 (4B7)
OFF6 (4B7)
OFF5 (4B7)
U18 4094
OFF4 (4B7)
OFF3 (4B7)
OFF2 (4B7)
OFF1 (4B7)
AMP10 (4C6)
AMP9 (4C6)
AMP8 (4C7)
AMP7 (4C7)
U19 4094
AMP6 (4C7)
AMP5 (4C7)
AMP4 (4C7)
AMP3 (4C7)
AMP2 (4C7)
AMP1 (4C7)
A0 (4B3)
A1 (4B2)
U28B 1/2 HC390
INTREF (3B4)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, PLL/WAVEFORM BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		MODEL NO 75
	DO NOT SCALE DWG		DWG NO 0103-00-1456
	SCALE		REV D
			CODE IDENT 23338
			SHEET 2 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27286

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REV	ECN	BY	DATE	APP

TRIGGER AND HOLD LOGIC

TRIG IN J18 — CR1, CR2, R16 100K — HCT04 U12B — U15B HC86 — P5B-3 SLOPE

U24B 1/2 HC74 (SET, CLK, D, CLR)

U15C HC86 — TGL (2A7)

U26D HC00 — U26A HC00

GATE (2A7) — U21B HCT00

U23B 1/2 HC74 — (2A7) CONT — J9-15 TRIGMASK — BURLOAD J9-11

U23A 1/2 HC74 — J7-19 CLK (B6)

HOLD IN (J24) P5A-1 — R18 100K, CR5, CR6 — HCT04 U12F — HC04 U25C

SYNC IN J20 — CR8, CR7, R19 100K — (C7) SYNCEN — U21A HCT00 — SYNC IN J9-14

RETURN IN (J25) P5A-2 — CR9, R20 100K, CR10 — U12E HCT04 — ATS P5A-4

P58-4 MANHOLD — AS08 U27B

U21D HCT00 — (2A7) BURST, J9-16 STOPOK, J9-13 TPOINT — AS10 U22C — RN3 6.8K — STOPNOW (B7)

U24A 1/2 HC74 — P5B-8 ARB R/W, J7-17 FB — NO LOAD J9-20

U27A AS08 — U17A AS10 — U17B AS10 — U22B AS10

U20A HC00 — (D5) GATE, (C6) BURST — SYNCEN (D1)

U20B HC00 — U17C AS10 — U27D AS08 — J7-19 CLK (B1)

BDO (B6) — U25A HC04 — U25B HC04 — BURST DONE OUT J19

U26B HC00 — U27C AS08 — RN3 6.8K

U16A HC00 — U16D HC00 — U22A AS10 — RN3 6.8K

U16B HC00 — U15D HC86 — J9-12 PCLK 13 — CLK (C5) J7-19

P5A-9 REF IN (J27) — CR3, CR4, R17 100K — U12D HCT04 — U16C HC00 — U25E HC04

(2B7) REFSEL — U26C HC00 — INTREF (2B2) — U25D HC04 — U21C HCT00

U15A HC86 — U25F HC04 — REF OUT (J28) P5A-10

WAVEFORM LATCH

U1, U3 HC374 (CLK, OC)

	U1		U3	
J7-15	ZBIT	WF12 (4D7)	WBIT3	WF3 (4D8)
J7-12	WBIT12	WF11 (4D7)	WBIT6	WF6 (4D7)
J7-11	WBIT11	WF9 (4D7)	WBIT10	WF10 (4D7)
J7-9	WBIT9	BDO (C4)	WBIT7	WF7 (4D7)
(C5)	STOPNOW	STOP P5A-7	WBIT8	WF8 (4D7)
J7-13	STBIT		WBIT5	WF5 (4D7)
J7-14	SBIT		WBIT4	WF4 (4D7)
J7-1	WBIT1	WF1 (4D8)	WBIT2	WF2 (4D8)

SYNC OUT J21 — HCT04 U12A

U20C HC00 — U20D HC00 — U12C HCT04

Z-AXIS DRIVER

Q1–Q6 2N3904

CR11 (ZL2 2A7), CR12 (ZL1 2B7), CR13 (ZL0 2B7)

R21 1.1K, R22 2.21K, R23 4.64K

C12 10pF, R24 49.9K, R25 2K, C13 330pF, R28 2K, R29 1.21K, R30 1.21K

R26 61.9K, R27 2.37K

+15, -15

Z-AXIS (J26) P5A-3

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, PLL/WAVEFORM BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75 — DWG NO 0103-00-1456 — REV D
	SCALE		CODE IDENT 23338 — SHEET 3 OF 4

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REV	ECN	BY	DATE	APP

WAVEFORM SYNTHESIZER

SUM IN J22, F1 1/4A FB, CR15 5.1V 1N751A, CR14 5.1V 1N751A, R34 50 1W .25%

U2 AD565AJD: WF1 (3B6) … WF12 (3B6) → DI1 … DI12; DGND; RIN; AGND; ROUT; VDD; VSS; OFFSET; 10V SPAN; 20V SPAN; DAC OUT

R31 42.2, R32 46.4, C14 .1, C15 .1, C16 15pF, R33 1.62K, C17 .1, C18 .1, C19 .1, C20 100 25V

U6 LT318A, C21 .1, C22 100 25V

RN1 2K, 909, 2.5K, 5K; C23 .1

U7 LT318A, C24 .1, C25 .1, C26 .1

OUTPUT AMPLIFIER

R36 499, R37 8.25K, C40 4700pF, C41 .1

U10 LF411CN, C42 .1

R38 432, RN2 500 / 1.25K / 625, C43 120pF

Q7 2N3906, Q8 2N3904, Q9 2N2219A, Q10 2N2905A

R39 2K, R40 13K, R41 13K, R42 2K, R43 100, R44 33.2, R45 33.2, R46 33.2, R47 100

R48 61.9K, R49 8.25K, R50 10 1/2W, R51 10 1/2W, R52 10 1/2W, R53 10 1/2W

RN2 1.28K / 1.28K, C50 10pF, C51 1500pF, C52 22pF

CR16 1N4002, CR17, CR18 1N4002, CR19 1N4002

C44 .01, C45 .01, C46 .1, C47 100 25V, C48 .1, C49 1, C53 .1, C54 1, C55 .1, C56 100 25V, C57 .1, C58 100 25V, C59 .1, C60 100 25V

PA OUT (B4)

AMPLITUDE CONTROL

U9 AD7240JN: AMP1 (2A3) … AMP10 (2A4) → DI1 … DI12; VREF; VOUT; RBIAS; AGND; DGND; VDD

C28 .1, C27 .1

U8 LT318A, C29 .1, C30 100 25V, C31 .1, C32 100 25V, R35 4.99K, C33 33pF

RN2 610

OFFSET CONTROL

U5 AD7240JN: OEF12 (2B5) … OEF1 (2A4) → DI12 … DI1; VOUT; VREF; VDD; DGND; AGND; RBIAS

C34 .1, C35 150pF

U4 LF411CN, C36 .1, C37 .1

ATTENUATOR

PA OUT (C1), R54 4.99K .1%, R55 499 .1%, R56 56.2, R57 100 1W .25%, R58 100 1W .25%, R59 10, R60 12.4

K1, K2, Q11 2N3904, Q12 2N3904, R61 3.01K A0 (2A3), R62 3.01K A1 (2A3)

F2 1/2A FB, 50 Ω OUT J23

CR20 1N5349A 12V, CR21 12V 1N5349A

SHIFTED LOGIC POWER SUPPLY

VR1 79L05, C38 100 25V, VR2 78L15, C39 100 25V

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC, PLL/WAVEFORM BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75 · DWG NO 0103-00-1456 · REV D
	SCALE		CODE IDENT 23338 · SHEET 4 OF 4

BISHOP GRAPHICS ACCUPRESS REORDER NO A27085

REV	ECN	BY	DATE	APP
B	FOR RELEASE		7/23/85	
C	7386		5/6/86	

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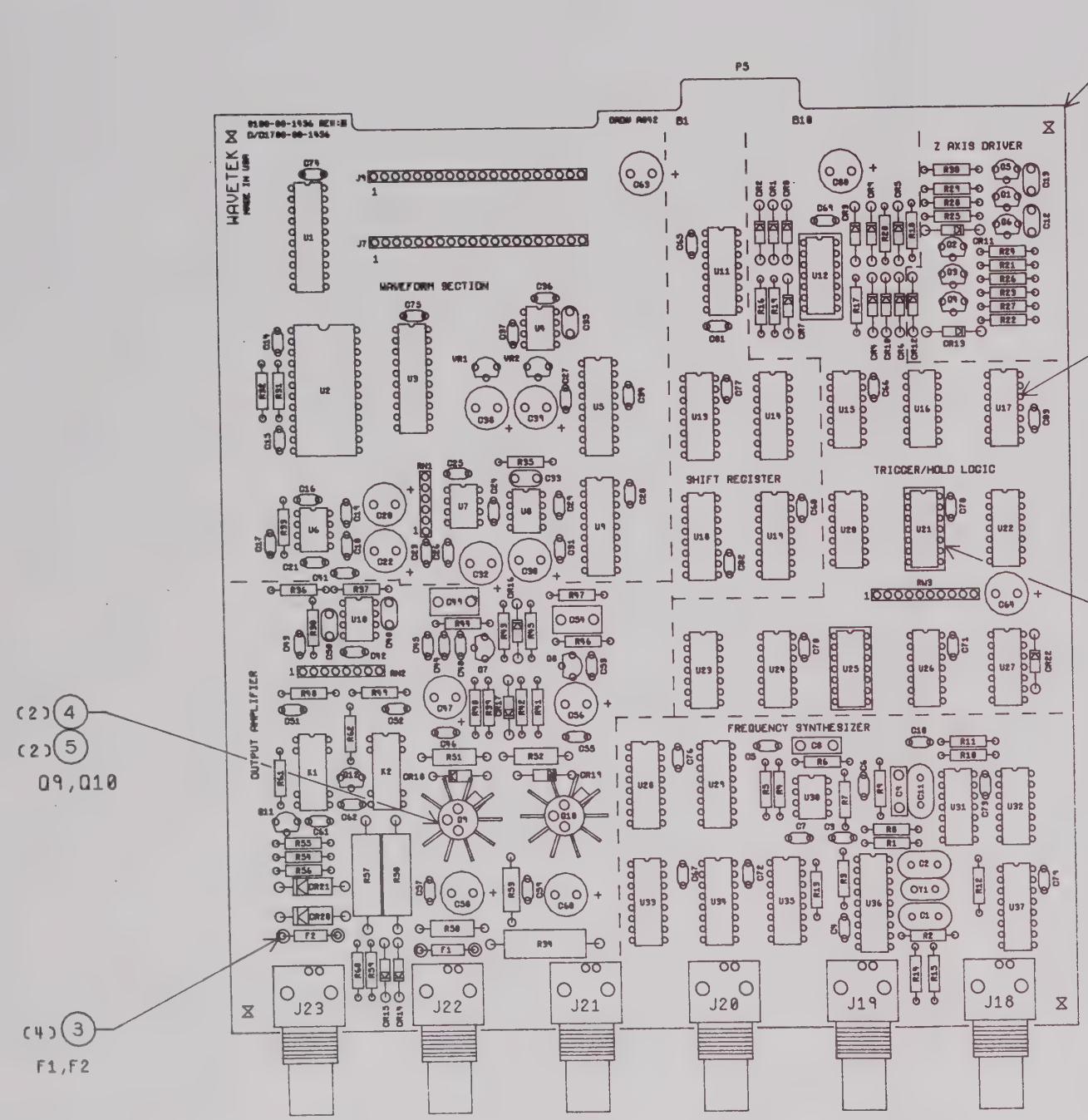

1 (TYP)

2 (3)
U12,U21 U25

(2) 4
(2) 5
Q9,Q10

(4) 3
F1,F2

3. FOR ASSEMBLY INTERCONNECTION, SEE INSTRUMENT SCHEMATIC 0004-00-0366.

2. SEE 0103-00-1456 FOR SCHEMATIC.

1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A1 A1 A3.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST 1100-00-1456

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 3-5-86	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ MGR	2-24-75	TITLE: PCA, PLL/WAVEFORM
FINISH WAVETEK PROCESS —	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 75
	SCALE NONE		DWG NO. 1100-00-1456 REV C
			CODE IDENT 23338 SHEET 7 OF 1

1100-00-1456 C

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PCA PLL WAVEFORM BD	0103-00-1456	WVTK	0103-00-1456	1
C12	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C50	CAP, CER, DISC, 10PF, 1KV, COG, 5%, RAD LD .25	10TCG10	SPRAG	1500-01-0031	1
C44 C45	CAP, CER, MN, .01MF, 50V Z5U, +80/-20% RAD LEAD .2	1C20Z5U103M050B	SPRAG	1500-01-0311	2
C10 C14 C15 C17 C18 C19 C21 C23 C24 C25 C26 C27 C28 C29 C3 C31 C34 C36 C37 C4 C41 C42 C46 C48 C5 C53 C55 C57 C59 C6 C61 C62 C65 C66 C67 C68 C69 C7 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C81 C82 C83	CAP, CER, MN, .1MF, 50V, Z5U, +80/-20% RAD LD SP .2	5028E550RD104Z	KYCRA	1500-01-0420	51
C43	CAP, CER, MN, 120PF, 50V COG, 5%, RAD LD .2	5028E050RD121J	KYCRA	1500-01-2100	1
C16	CAP, CER, MN, 15PF, 50V, COG, 5% RADIAL LEAD SP .2	5028E050RD150J	KYCRA	1500-01-5003	1
C35	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1
C51	CAP, CER, MN,	5028E050RD152J	KYCRA	1500-01-5200	1

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	1500PF, 50V, COG, 5%, RAD LD .2				
C52	CAP, CER, MN, 22PF, 50V, COG, 5%, RADIAL LD SP .2	5028E050RD220J	KYCRA	1500-02-2016	1
C33	CAP, CER, MN, 33PF, 50V, COG, 5%, RAD LD .2	5028E050RD330J	KYCRA	1500-03-3020	1
C13	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C40	CAP, CER, MN, 4700PF, 50V, COG, 5%, RAD LEAD SP .2	5028E050RD472J	KYCRA	1500-04-7203	1
C11	CAP, MICA, 15PF, 500V	DM15-150J	ARCO	1500-11-5000	1
C1 C2	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C20 C22 C30 C32 C38 C39 C47 C56 C58 C60 C63 C64 C80	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	13
C49 C54	CAP, MET, POLY, 1MF, 63V, 5% RAD LD SP .3	167/1/J/63/D	WEST	1500-41-0513	2
C8	CAP, MET, POLY, .1MF, 63V, 5% RAD LEAD SP .3	167/.1/J/63/A	WEST	1500-43-0413	1
C9	CAP, MET, POLY, .033MF, 100V, 5% RAD LEAD SP .3	167/.033/J/100/A	WEST	1500-43-3314	1

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
1	DRILL DRWG, PLL WAVEFORM BD	1700-00-1456	WVTK	1700-00-1456	1
J18 J19 J20 J21 J22 J23	CONNECTOR, BNC(PC)	227161-1	AMP	2100-01-0019	6
J7 J9	HEADER, CONN(20 PIN)	643119-1	AMP	2100-02-0151	2
.2	SKT, IC, 14 PIN	DILB14P/108	BURND	2100-03-0066	3
3	SOCKET, MINISERT	75060-012	BERG	2100-03-0076	4
Y1	CRYSTAL, 6.144 MHZ	MP-1	MTRON	2300-00-0014	1
F2	FUSE, 1/2A, 125V(PC)	255.500	LITFU	2400-05-0035	1
F1	FUSE, 1/4, 125V (PC))	255.250	LITFU	2400-05-0042	1
4	HEAT SINK	207	WAKE	2800-11-0001	2
5	TRANSIPAD	333-125-NY	BLINN	2800-11-0017	2
K1 K2	RELAY, FORM C, DIP	RA30441051-02	ETROL	4500-00-0018	2
R50 R51 R52 R53	RES, C, 1/2W, 5%, 10	RC-1/2-100J	STKPL	4700-25-0100	4
R55	RES, MF, 1/8W, .1% T2 499	CMF-1/10B(T-9)499	DALE	4701-02-4990	1
R54	RES, MF, 1/8W, .1% T2 4.99K	CMF-1/10B(T-9)4.99K	DALE	4701-02-4991	1
R2 R43 R47	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	3

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R10	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
R1 R12 R13 R4 R5	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	5
R16 R17 R18 R19 R20	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	5
R59	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	1
R21	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	1
R29 R30	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	2
R60	RES, MF, 1/8W, 1%, 12.4	RN55D-12R4F	TRW	4701-03-1249	1
R40 R41	RES, MF, 1/8W, 1%, 13K	RN55D-1302F	TRW	4701-03-1302	2
R33	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	1
R3	RES, MF, 1/8W, 1%, 16.5K	RN55D-1652F	TRW	4701-03-1652	1
R25 R28 R39 R42	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	4
R14 R15 R7	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R22	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R27	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R8	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R61 R62	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	2
R9	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R44 R45 R46	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R11	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R31	RES, MF, 1/8W, 1%, 42.2	RN55D-42R2F	TRW	4701-03-4229	1
R38	RES, MF, 1/8W, 1%, 432	RN55D-4320F	TRW	4701-03-4320	1
R23	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	1
R32	RES, MF, 1.8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	1
R36	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R35	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R24	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R56	RES, MF, 1/8W, 1%, 56.2	RN55D-56R2F	TRW	4701-03-5629	1
R26 R48	RES, MF, 1/8W, 1%, 61.9K	RN55D-6192F	MEPCO	4701-03-6192	2
R6	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	1
R37 R49	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	2
R57 R58	RES, MF, 1W, .25%, T2 100	MFS1/2100RCT2	DALE	4701-38-1000	2
R34	RES, MF, 1W, .25%, T2 50	MFS1/250RCT2	DALE	4701-38-5009	1

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
RN3	RES MODULE	4310R-101-682	BOURN	4770-00-0016	1
RN1	RES MODULE, CUSTOM	4770-00-0044	WVTK	4770-00-0044	1
RN2	RES MODULE, CUSTOM	4770-00-0046		4770-00-0046	1
CR14 CR15	DIODE	1N751A	FAIR	4801-01-0751	2
CR22	DIODE, 6.2V, 10%, 1W, ZENER	1N4735	MOT	4801-01-4735	1
CR20 CR21	DIODE	1N5349A	MOT	4801-01-5349	2
CR18 CR19	DIODE	1N4002	FAIR	4801-02-0001	2
CR1 CR10 CR11 CR12 CR13 CR16 CR17 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	15
Q9	TRANS	2N2219A	NSC	4901-02-2191	1
Q10	TRANS	2N2905A	NSC	4901-02-9051	1
Q1 Q11 Q12 Q2 Q3 Q4 Q5 Q6 Q8	TRANS	2N3904	FAIR	4901-03-9040	9
Q7	TRANS	2N3906	FAIR	4901-03-9060	1
U30	IC	CA082E	RCA	7000-00-8200	1
U6 U7 U8	IC	LT318AN8	LINTE	7000-03-1802	3
U10 U4	IC, LOWOFFSET/DRIFT	LF411CN	NSC	7000-04-1100	2

WAVETEK PARTS LIST | TITLE: ASSY, PLL WAVEFORM BD | ASSEMBLY NO. 1100-00-1456 | REV C | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, PLL WAVEFORM BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 75 / DWG NO 1100-00-1456 / REV C
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 2
	SCALE		

BISHOP GRAPHICS/ACCUPRESS REORDER NO A27088

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	JFET INPUT OPERATIONAL AMPL				
U2	IC, 12 BIT MON D/A CONVERTER	AD565AJD	ANDEV	7000-05-6501	1
U5 U9	IC, 12-BIT VOLTAGE DAC	AD7240JN	ANDEV	7000-72-4000	2
VR2	IC	78L15	TI	7000-78-1501	1
VR1	IC, 3 TERMINAL NEG 5V REGULATOR	LM79L05ACZ	NSC	7000-79-0501	1
U11	IC, TRIPLE 2 CHANNEL MUX\DEMUX	CD4053BC	NSC	8000-40-5300	1
U13 U14 U18 U19	IC	CD4094BE	RCA	8000-40-9400	4
U16 U20 U26	IC, QUAD 2-INPUT NAND	8000-74-0011	WVTK	8000-74-0040	3
U21	IC, QUAD, 2 INPUT NAND	CD74HCT00	RCA	8000-74-0042	1
U25	IC, HEX INVERTER	MM74HC04	NSC	8000-74-0440	1
U12	IC, HEX INVERTER	MM74HCT04	NSC	8000-74-0441	1
U27	IC, QUAD 2-INPUT POS-NAND GATES	SN74AS08	TI	8000-74-0820	1
U17 U22	IC, TRIPLE 3 INPUT NAND	SN74AS10	TI	8000-74-1020	2

WAVETEK PARTS LIST	TITLE: ASSY, PLL WAVEFORM BD	ASSEMBLY NO. 1100-00-1456	REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U23 U24	IC, DUAL FLIP-FLOP	74HC74	MOT	8000-74-7440	2
U32	IC, JK FLIP-FLOP	MM74HC107	NSC	8007-41-0740	1
U29 U37	IC,	74HC151	TI	8007-41-5140	2
U1 U3	OCTAL D-FLIP FLOP, HCMOS, TRISTATE 20 PIN DIP	74HC374	TI	8007-43-7440	2
U28 U33 U34 U35	IC, DECADE COUNTER	MM74HC390	NSC	8007-43-9040	4
U31	IC	74LS624	TI	8007-46-2410	1
U15	IC, QUAD 2-INPUT EXCLUSIVE OR	74HC86	MOT	8007-74-8640	1
U36	IC, SERIAL INPUT PLL FREQ SYNTH.	MC145155	MOT	8100-00-0007	1

WAVETEK PARTS LIST	TITLE: ASSY, PLL WAVEFORM BD	ASSEMBLY NO. 1100-00-1456	REV C

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST ASSY, PLL WAVEFORM BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		MODEL NO 75 / DWG NO 1100-00-1456 / REV C
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 2 OF 2
	SCALE		

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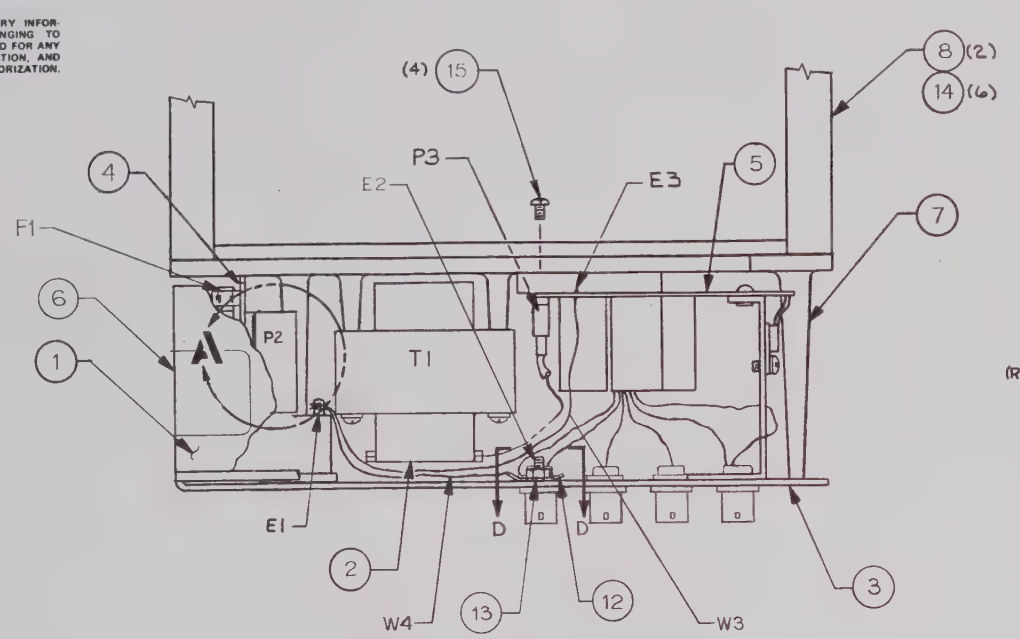
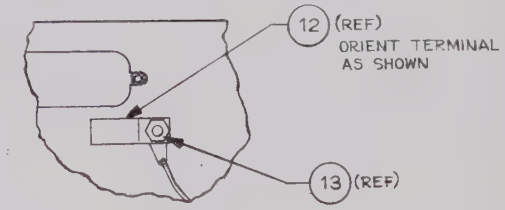
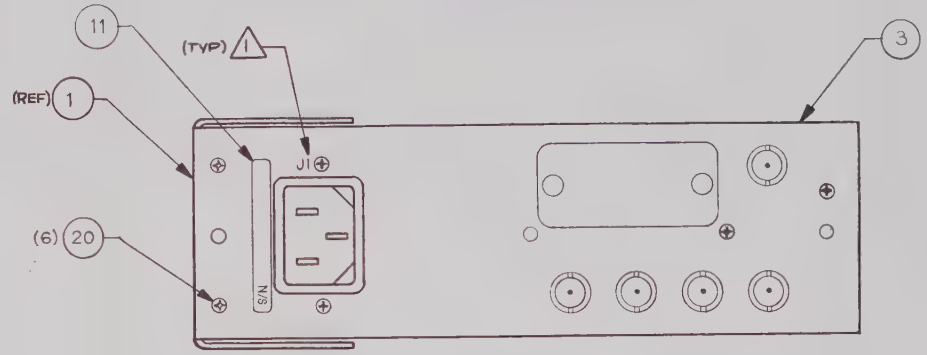
REV	ECN	BY	DATE	APP
A	14946, 7386	[illegible]	5-6-86	A.P.T.

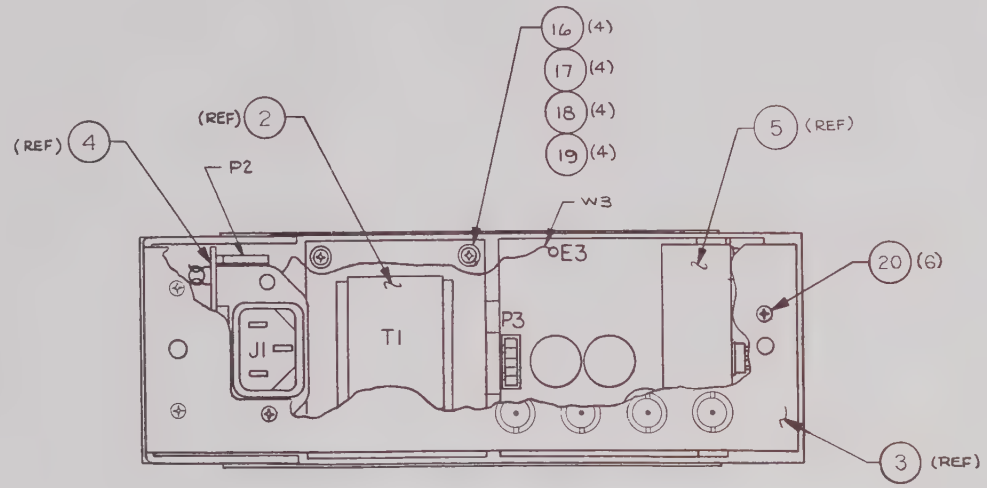


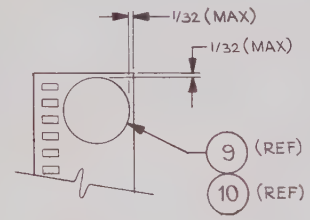


VIEW D-D



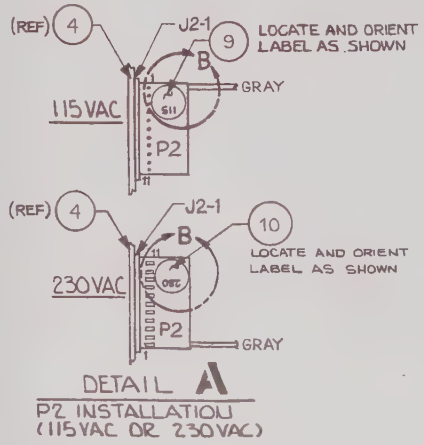
LABEL INSTALLATION





DETAIL B
SCALE 2/1

DETAIL B
SCALE 2/1



DETAIL A
P2 INSTALLATION
(115 VAC OR 230 VAC)

4. WIRES & CABLES OBTAINED FROM CABLE KIT 1207-00-1777.
3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-0366.
2. SEE 0103-00-1113 FOR SCHEMATIC.
⚠ REFERENCE DESIGNATIONS DO NOT APPEAR ON ACTUAL PARTS.

NOTE: UNLESS OTHERWISE SPECIFIED

DETAIL 'A'

WIRING LIST			
FROM	TO	REF DES	
E1	E2	W4	
E1	E3	W3	
P2 (1 THRU 11)	J2 (1 THRU 11)	—	115 VAC
P2 (11 THRU 1)	J2 (1 THRU 11)	—	230 VAC
P3 (1 THRU 5)	J3 (1 THRU 5)	—	

SEE SEPARATE PARTS LIST 1101-00-1771

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A.TALMADGE	DATE 3/7/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY, POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: .010 ANGLES: 1° XX: .030		
	DO NOT SCALE DWG		MODEL NO 75 / DWG NO 1101-00-1771 / REV A
	SCALE 1/1 & NOTED		CODE IDENT 23338 / SHEET 1 OF 1

1101-00-1771 A

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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REV	ECN	BY	DATE	APP
B	# 4668, 4707	A.T.	3/4/83	A.R.T.
C	#4728	KA	9/10/85	A.R.T.
D	#6028	DAH	2/11/86	A.R.T.

A2 A2
PCA AC PRIMARY
1208-00-1119

F1		
MODEL	115	230
21/22	3/8 A	3/16 A
23	1/2 A	1/4 A
75	3/8 A	3/16 A

NOTE FOR 230V HOOK-UP INVERT CONNECTOR P2 AS SHOWN BELOW

J2-	P2-
1	11
2	10
3	9
4	8
5	7
6	6
7	5
8	4
9	3
10	2
11	1

A2 A1
PCA POWER SUPPLY
1208-00-1118 (MODEL 21/22/23)
1208-00-1772 (MODEL 75)

J32 1 2 3 4 5 6 7

OFF ④ F1 ON S1

J1 HOT NEUT GND

E1

(115V HOOK-UP) J2- P2-
1 N.C. 2 N.C. 3 N.C. 4 N.C. 5 N.C. 6 7 N.C. 8 9 10 11

A2 T1
BLK WHT/BLK GRY WHT/GRY
RED WHT/RED RED BLU BLU

P3- J3-
2 3 1 5 4

CR1 VM18
C1 .01 GAP
C2 1000/50V
C3 1000/50V
C4 4.7/50V
C5 4.7/50V
C6 .1/50V
C7 10/25V
C8 10/25V
VR1 LM325A OR LM125
R1 ③
R2 ③
Q1 TIP29
Q2 TIP29
+15V
-15V

C9 .01 GAP
CR2 VSB54
C10 2200/16V
VR2 LM7805 IN OUT COM
C11 .1
C12 .1
+5V

RV1 V56ZA8

(W3) GRN/YEL E3
GRN/YEL (W4) E2

J4- A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8 A9 B9 A10 B10
-15V
+5V
+15V
J5- A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8 A9 B9 A10 B10
J31 1 2 3 4 5 6

P32 1 2 3 4 5 6 7 8 9 10 11
BLK ORN WHT/BLK GRY VIO WHT/GRY
P3 2 3 1 5 4
P2 1 2 3 4 5 6 7 8 9 10 11

CONNECTIONS FOR TRANSFORMER WITH HI/LO AND 115/230V PRIMARIES
(SHOWN IN 115V, HI POSITION – REVERSE P32 FOR LO POSITION)

④ FOR FUSE P/N SEE:
MODEL 21/22-1101-00-1113
MODEL 23-1101-00-1703
MODEL 75-1101-00-1771

③ R1 AND R2 VALUES:
10, 1/4W (MODEL 21/22/23).
1.5Ω, 1/2W (MODEL 75)

2. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2.

NOTE: UNLESS OTHERWISE SPECIFIED

0103-00-1113 E010

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 5/3/82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR	10/4/83	TITLE SCHEMATIC, POWER SUPPLY (A2)
FINISH WAVETEK PROCESS —	RELEASE APPROV	11/4/83	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 21/22 DWG NO 0103-00-1113 REV D
	SCALE —		CODE IDENT 23338 SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3884

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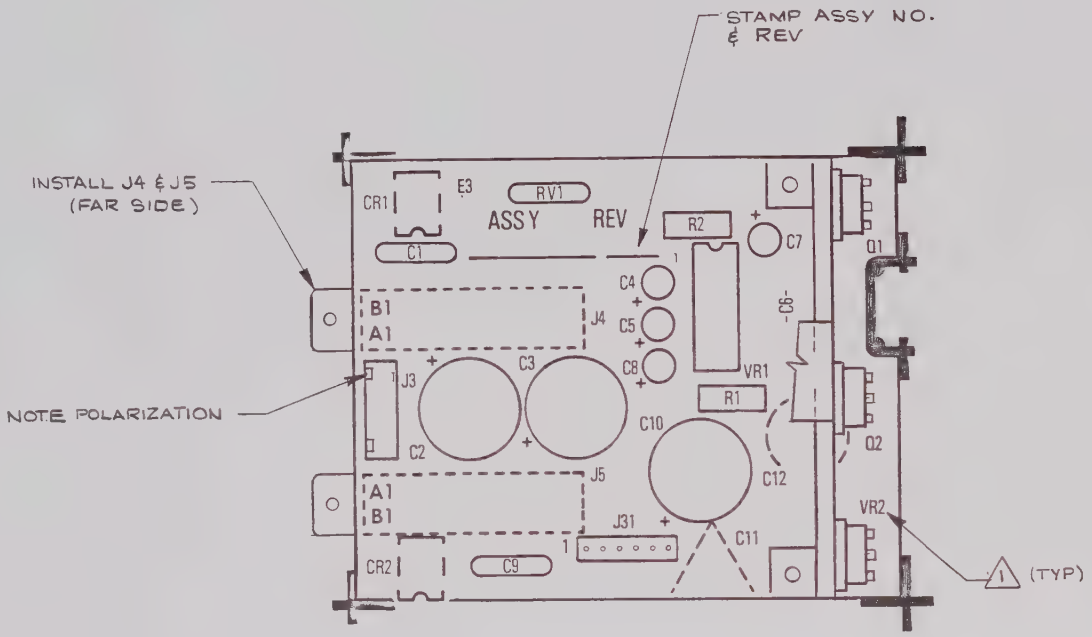
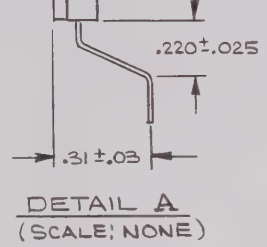
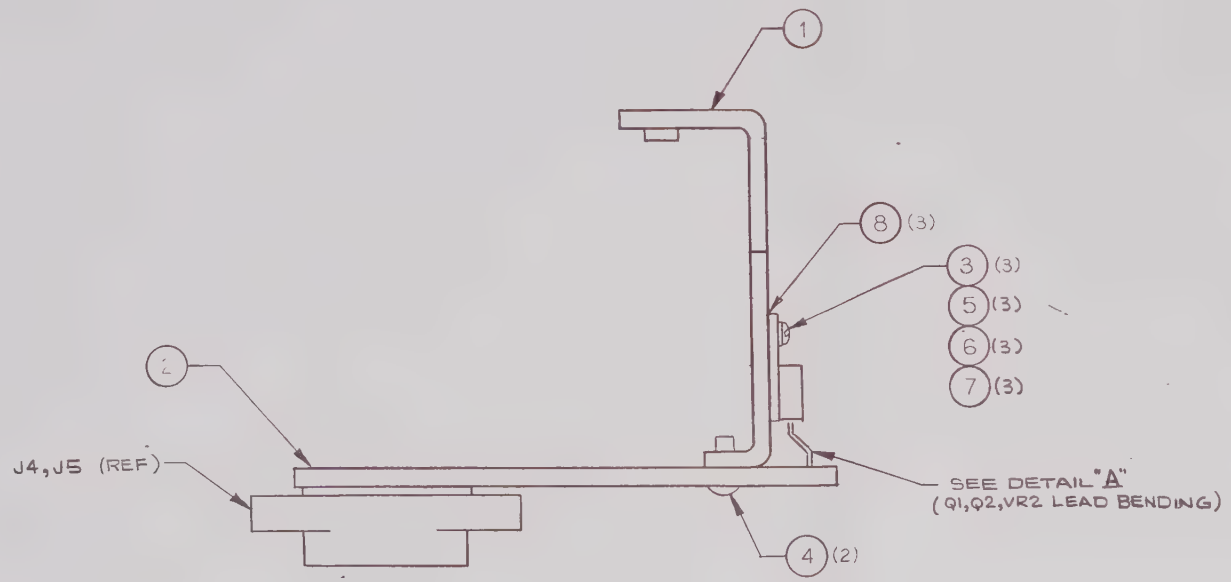
REV	ECN	BY	DATE	APP





DETAIL A
(SCALE: NONE)



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
NONE	ASSY, HEATSINK BRKT	75-2251	WVTK	1206-00-2251	1
C1 C9	CAP, CER, .01MF, 1KV	QAP-103	CRL	1500-01-0309	2
C11 C12 C6	CAP, CER, MN, .1MF 50V, Z5U, +80/-20% RADIAL LEAD SP .2	5028ES50RD104Z	KYCRA	1500-01-0420	3
C7 C8	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	2
C2 C3	CAP, ELECT, 1000MF/50V RADIAL LEAD, SP .30	CRE SERIES 1000/50	CAPAR	1500-31-0203	2
C10	CAP, ELECT, 2200MF, 16V RADIAL LEAD, SP .30	CRE SERIES 2200/16	CAPAR	1500-32-2201	1
C4 C5	CAP, ELECT, 4.7MF/50V RADIAL LEAD, SP .10	CLE SERIES 4.7/50	CAPAR	1500-34-7903	2
2	POWER SUPPLY BD	21-1118	WVTK	1700-00-1118	1
J4 J5	CONNECTOR(20 PIN)	ETCIODRTI	SULIN	2100-02-0139	2
J3	HEADER, CONN(5 PIN)	102202-2	AMP	2100-02-0143	1
J31	CONN, HEADER, 6 PIN	640098-6	AMP	2100-02-0170	1
3	WASHER	B51547F015	MOT	2800-11-0015	3
4	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	2
5	SCREW, SELF TAPPING TYPE B, PAN CROSS RECESS, 4-40X3/8	4-24 X 3/8	CMRCL	2800-22-4162	3
6	WASHER, FLAT, 4(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	3
7	WASHER, SPLIT LOCK, 4	#4SRLW	CMRCL	2800-42-4000	3
8	INSULATOR(TO-220)	60-11-8302-1674	CHOMR	3100-00-0010	3
R1 R2	RES, CAR, 1/2W, 5%, 1.5	RC20GF1R5J	STKPL	4700-25-0159	2
RV1	VARISTOR	4799-00-0048	WVTK	4799-00-0048	1
CR1 CR2	DIODE, BRIDGE	VM18	VARO	4801-02-0008	2
Q1 Q2	TRANS	TIP-29	TI	4902-00-0290	2
VR1	IC, VOLTAGE REGULATOR	LM325A	NSC	7000-03-2501	1
VR2	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-
2. SEE 0103-00-1771 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A1.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. Redman	DATE 9/28/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PCA, POWER SUPPLY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ±.010 ANGLES ±1, XX ±.030		
	DO NOT SCALE DWG		
	SCALE 2/1	MODEL NO 75	DWG NO 1208-00-1772 REV
		CAGE NO 23338	SHEET 1 OF 1

1208-00-1772

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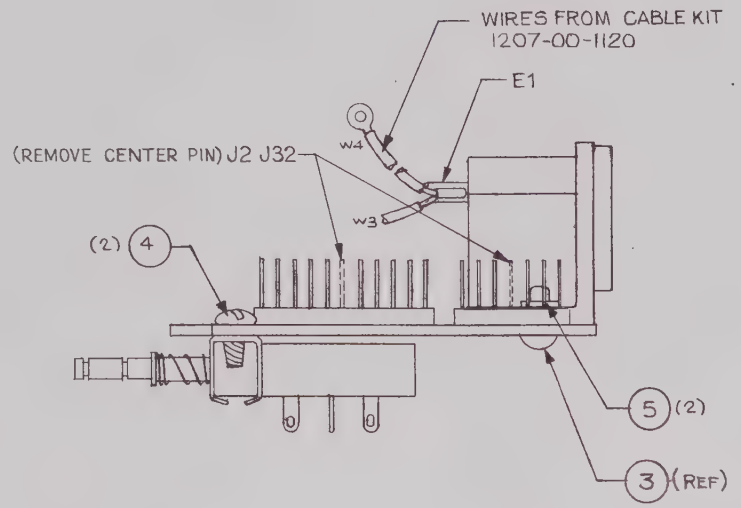
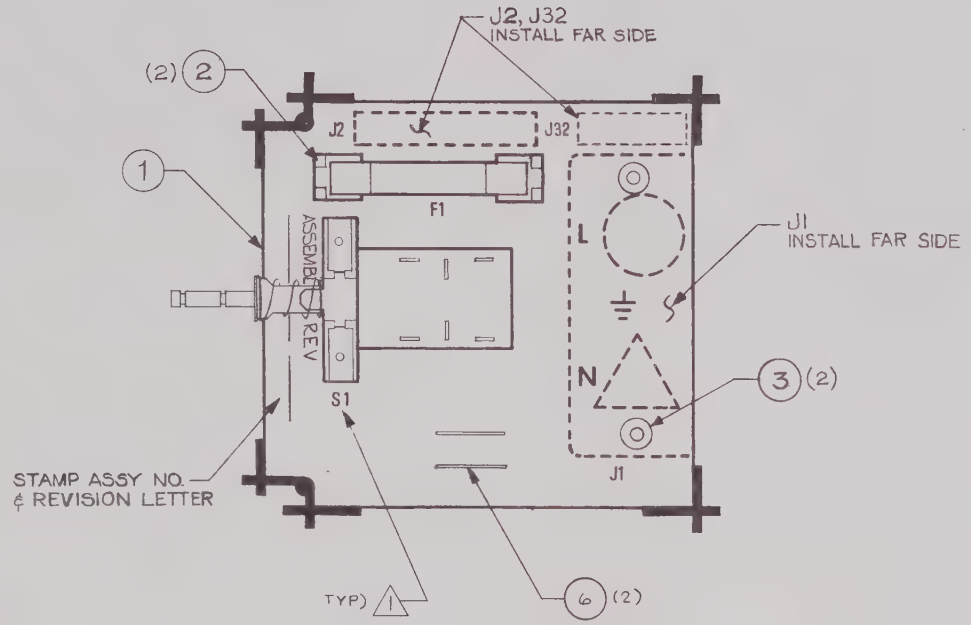
REV	ECN	BY	DATE	APP
A	#125|4546|4250	KA	1/14/85	A.E.T.
	#4595	KA	4/25/85	A.E.T.





REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, PWR SUP	0103-00-1113	WVTK	0103-00-1113	1
1	AC PRIMARY BD	21-1119	WVTK	1700-00-1119	1
J2	HEADER, CONN(11 PIN)	1-87224-1	AMP	2100-02-0144	1
J32	CONN, HEADER, UNSHROUDED, 7 PIN	87224-7	AMP	2100-02-0184	1
J1	RECEPT, POWER (PC)	EAC-303	SWCFT	2100-03-0069	1
2	FUSE HOLDER, CLIP	102071	LITFU	2400-05-0031	2
3	RIVET, ALUM 5/16X1/8 DIA .188-250	1125-0410	CHOBT	2800-12-0047	2
4	SCREW, S/T TYPE B, PAN CROSS RECESS, 4-24X1/4	4-24 X 1/4	CMRCL	2800-22-4142	2
5	WASHER, FLAT, 4(.312 O.D.)	#4FW	CMRCL	2800-26-4000	2
6	RESISTOR, 0 OHM JUMPER	JP02T6BQ	ROHM	4799-00-0087	2
S1	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST	TITLE: PCA, AC PRIMARY	ASSEMBLY NO.: 1208-00-1119	REV: B

PAGE 1

3. FOR ASSEMBLY INTERCONNECTION SEE INSTRUMENT SCHEMATIC 0004-00-1111.
2. SEE 0103-00-1113 FOR SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION A2A2.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: A TALMADGE	DATE: 6/13/83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL: —	PROJ ENGR:		TITLE: PCA, AC PRIMARY (A2A2)
	RELEASE APPROV:	11/4/83	
FINISH WAVETEK PROCESS: —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO: 21,22	DWG NO: 1208-00-1119 REV: B
	SCALE: 2/1	CODE IDENT: 23338	SHEET 1 OF 1

1208-00-1119 B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

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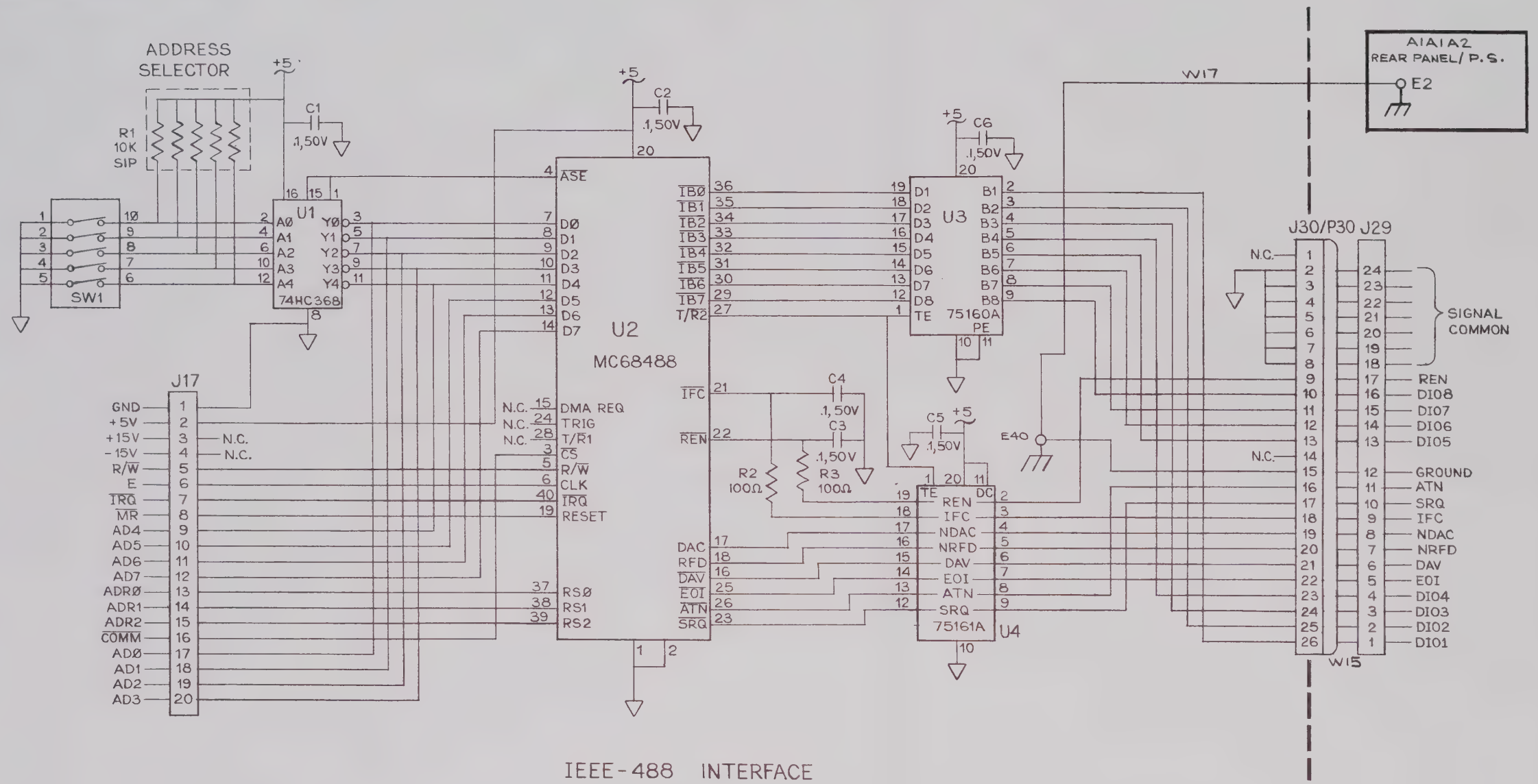

IEEE-488 INTERFACE

2. CAPACITOR VALUES ARE IN MICROFARADS (μF).
1. RESISTOR VALUES ARE IN OHMS, 1/8 WATT.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. TALMADGE	DATE 3/1/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL //	PROJ ENGR M. STEINER	8/26/85	TITLE SCHEMATIC, GPIB OPTION
FINISH WAVETEK PROCESS //	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 23/75 DWG NO. 0103-00-1678 REV
	SCALE //		CODE IDENT 23338 SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4831

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REV	ECN	BY	DATE	APP

5. ADDRESS SELECTOR SWITCH, FACTORY PRESET TO 9. SEE INSTRUMENT INSTRUCTION MANUAL.

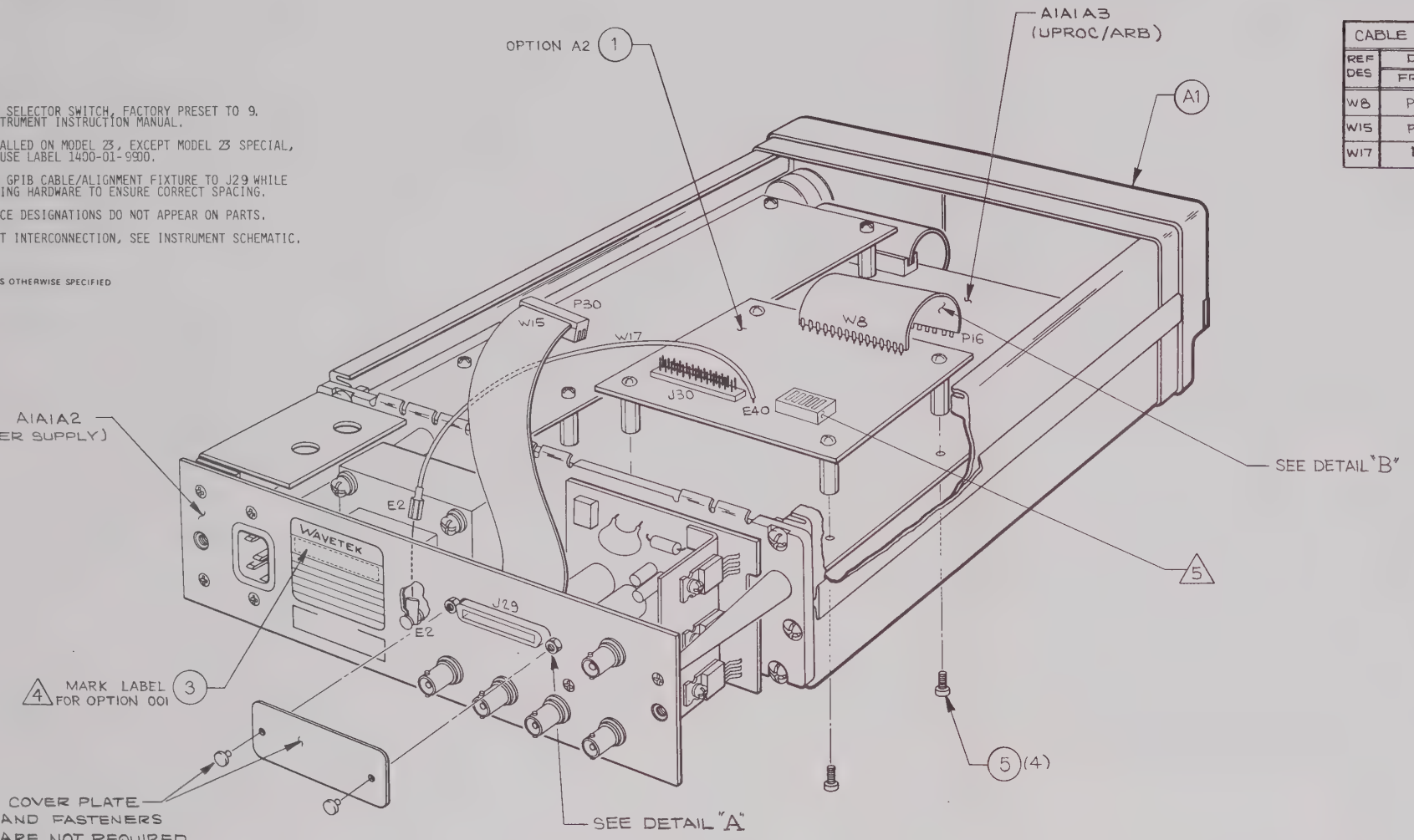
4. IF INSTALLED ON MODEL 23, EXCEPT MODEL 23 SPECIAL, DO NOT USE LABEL 1400-01-9900.

3. INSTALL GPIB CABLE/ALIGNMENT FIXTURE TO J29 WHILE TIGHTENING HARDWARE TO ENSURE CORRECT SPACING.

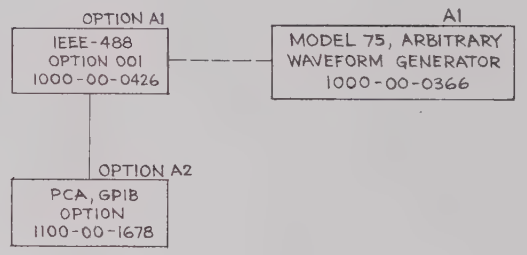
2. REFERENCE DESIGNATIONS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED



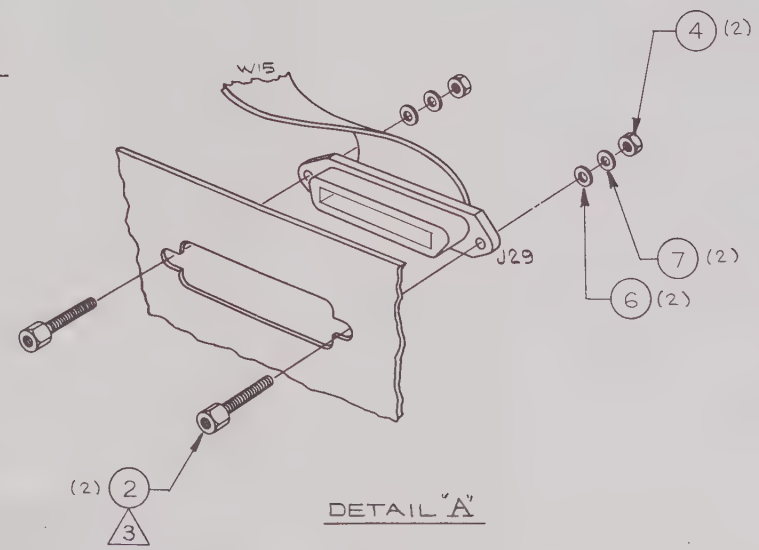
CABLE HOOKUP CHART		
REF DES	DESTINATION	
	FROM	TO
W8	P16	A1A1A3-J16
W15	P30	OPTION A1-J30
W17	E2	A1A1A2-E2



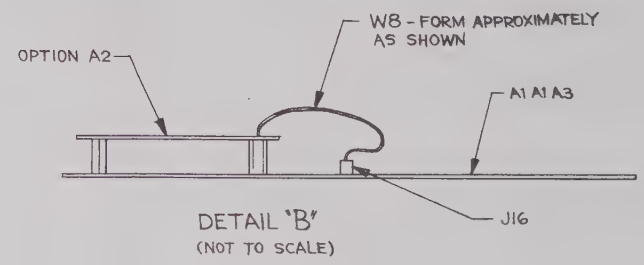
INSTRUMENT COVERS NOT SHOWN

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ACCEPTANCE TEST SPECIFICATION	23/75-0426	WVTK	0007-00-0426	1
1	PCA, GPIB OPTION	1100-00-1678	WVTK	1100-00-1678	1
2	JACK SCREW	859-0530	WVTK	1400-01-0530	2
3	LABEL, OPTION, MODEL 75	1400-01-9900	WVTK	1400-01-9900	1
4	NUT, HEX, CAD PLATE 6-32	MS35649-264	COML	2800-14-6100	2
5	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
6	WASHER, FLAT, #6 BIN 495	#6FLAT WASHER	CMRCL	2800-26-6001	2
7	WASHER, SPLIT LOCK #6 S	#6SRLW	CMRCL	2800-42-6000	2
W15	ASSY, GPIB RIBBON CABLE	6002-00-0030	WVTK	6002-00-0030	1

NOTE UNLESS OTHERWISE SPECIFIED



DETAIL "A"



DETAIL "B"
(NOT TO SCALE)

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 7/3/85	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR M. STEINER	8/24/85	TITLE IEEE-488 OPTION 001
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 23/75
	SCALE NONE		DWG NO 1000-00-0426 REV
			CODE IDENT 23338 SHEET 2 OF 2

BISHOP GRAPHICS, ACCUPRESS REORDER NO. A2708

1000-00-0426

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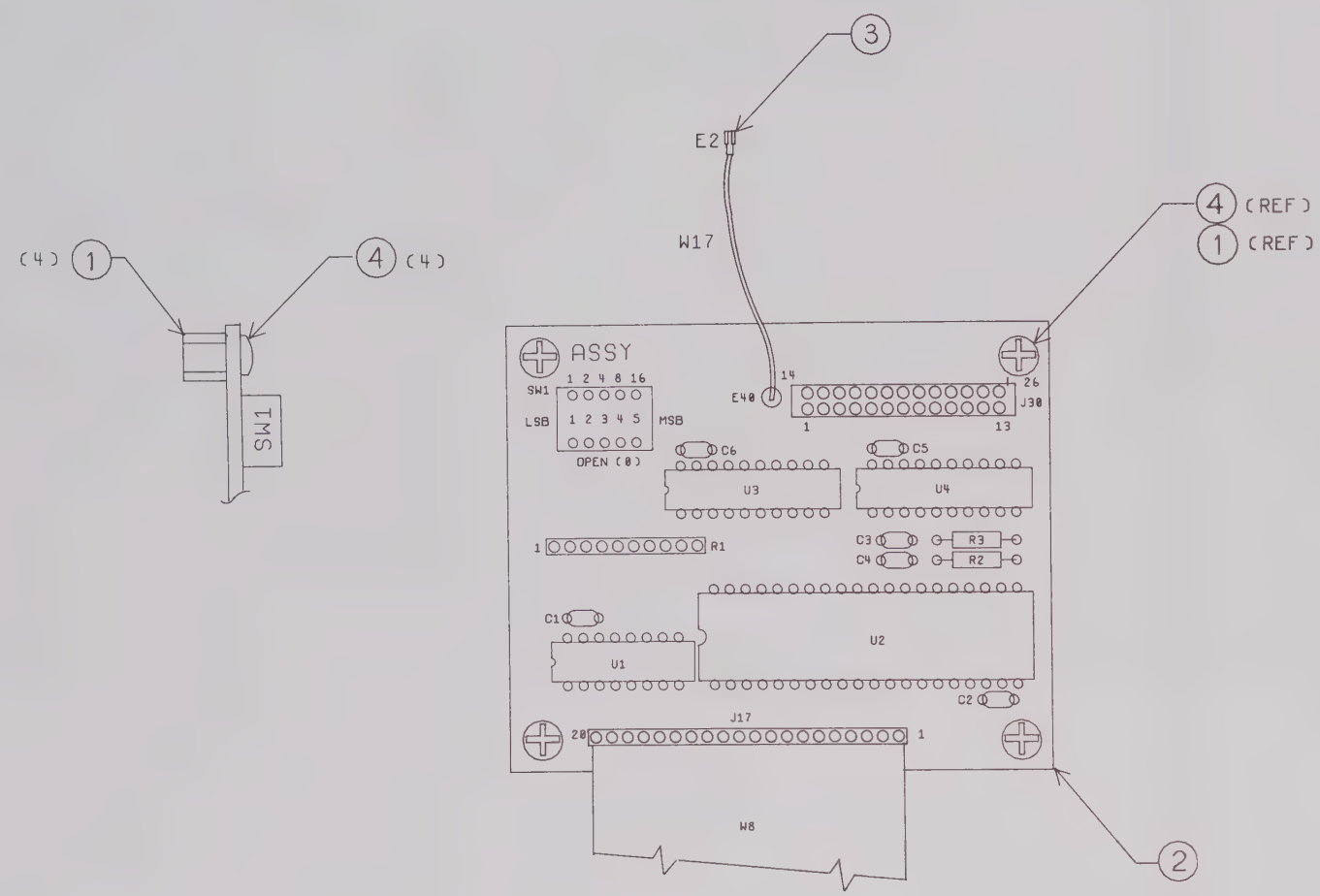
REV	ECN	BY	DATE	APP



CABLE HOOKUP CHART			
REF DES	AWG	LENGTH	COLOR
W17	18	5.0	GRN/YEL

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, GPIB OPTION	0103-00-1678	WVTK	0103-00-1678	1
1	STANDOFF	013-003-2	WVTK	1400-00-2503	4
C1 C2 C3 C4 C5 C6	CAP, CER, MN. . 1MF, 50V, Z 5U, +80/-20% RAD LD SP .2	5C2BE50RD104Z	KYCRA	1500-01-0420	6
2	GPIB OPTION BOARD	1700-00-1678	WVTK	1700-00-1678	1
J30	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	1
3	RECEPTACLE, QUICK DISCONNECT	60358-1	AMP	2100-04-0044	1
4	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
R2 R3	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R1	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	1
SW1	SWITCH PC	300-105	DUNCN	5199-00-0001	1
W17	WIRE, HU, 18GA	HH0603-0RN/YELLOW	JUDD	6000-31-6045	1
W8	CABLE, FLEXIBLE FLAT 2", 20 PIN	1-88665-9	AMP	6001-60-0008	1
U2	IC	MC68488P	MOT	~~8000-84-3800~~	1
U1	IC, HEX BUS DRIVER	SN74HC368	TI	8007-43-6840	1
U3	IC	75160	TI	8007-51-6000	1
U4	IC	SN75161N	TI	8007-51-6100	1

4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC FOR ASSEMBLY INTERCONNECTION.
2. SEE 0103-00-1678 FOR CIRCUIT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 5/3/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR N STEINER	5/16/85	TITLE PCA, GPIB OPTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 23/75
	SCALE 2/1		DWG NO 1100-00-1678 REV
			CODE IDENT 23338 SHEET 1 OF 1

1700-00-1678

BISHOP GRAPHICS/ACCUPRESS REORDER NO A2708

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REV	ECN	BY	DATE	APP

J17
GND → 1
+5 → 2
+15 → 3
-15 → 4
(C6) R/W → 5
(D6) E → 6
(C6) IRQ → 7
→ 8
(C6) AD4 → 9
(C6) AD5 → 10
(C6) AD6 → 11
(C6) AD7 → 12
(C6)ADR0 → 13
→ 14
→ 15
(D6) COMM → 16
(C6) AD0 → 17
(C6) AD1 → 18
(C6) AD2 → 19
(C6) AD3 → 20

U1 6850: VCC 12, CS0 8, CS1 10, CS2 9 (J17-16 COMM), E 14 (J17-6 E), R/W 13 (J17-5 R/W), RS 11 (J17-13 ADR0), D0 22 (J17-17 AD0), D1 21 (J17-18 AD1), D2 20 (J17-19 AD2), D3 19 (J17-20 AD3), D4 18 (J17-9 AD4), D5 17 (J17-10 AD5), D6 16 (J17-11 AD6), D7 15 (J17-12 AD7), IRQ 7 (J17-7 IRQ), VSS, TXD 6, RTS 5, RXD 2, CTS 24, DCD 23, TXCLK 4, RXCLK 3. C3 .1 to +5.

U2 HD-4702-9: VCC 16, CP 5, ECP 4, IX 7, OX 6, VSS 8, S0 14, S1 13, S2 12, S3 11, CO 9, IM 15, Z 10, Q0 1, Q1 2, Q2 3. C1 56pF, 2.4576MHz, R1 10M, C2 56pF, SW1 1-4. C4 .1 to +5.

U3 1488 (14/7): 12/13 → 11; 1/2 → 3; 4/5 → 6; 9/10 → 8.

U4 1489 RC (14/7): 2/3 → 1; 6/5 → 4; 9/8 → 10; 12/11 → 13.

C5 .1, C6 .1, C7 330pF, C8 470pF, C9 330pF, C10 470pF, C11 470pF, C12 .1 to +5.

CR1 1N5282 to +15; CR2 1N5282 to -15.

R2 49.9K, R3 6.04K.

DCE J30C P30 W15: 1 RXDATA, 2 TXDATA, 3 DTR/CTS, 4 RTS/DSR, 5 SIG GND, 6 RLSDC, 20 CTS/DSR.

DTE J30T P30 W15: 1 TXDATA, 2 RXDATA, 3 RTS/DSR, 4 CTS/DTR, 5 DSR, 6 SIG GND, 7 RLSDT, 20 DTR/CTS.

W15 1 TXD, 2 RXD, 3 RTS, 4 CTS, 5 DSR, 6 SIG GND, 7 RLSD, 20 DTR.

J29 W15 1-26.

U4 12 / 11 RC 1489 13

4. CAPACITORS VALUED IN MICROFARADS (uF).
3. RESISTORS VALUED IN OHMS, 1/8W.
2. FOR UNIT INTERCONNECTION, SEE INSTRUMENT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN PREFIX WITH APPROPRIATE ASSEMBLY REFERENCE DESIGNATION. (SEE INSTRUMENT SCHEMATIC)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 7/5/95
MATERIAL	PROJ ENGR	8/24/95
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC, RS-232 OPTION

MODEL NO	DWG NO	REV
23/75	0103-00-1677	A

CODE IDENT 23338 SHEET 1 OF 1

0103-00-1677 A

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REV	ECN	BY	DATE	APP

6. FACTORY CONFIGURED FOR DCE OPERATION. SEE INSTRUMENT INSTRUCTION MANUAL.

5. BAUD RATE SELECTOR SWITCH, FACTORY PRESET TO 9600 BAUD. SEE INSTRUMENT INSTRUCTION MANUAL.

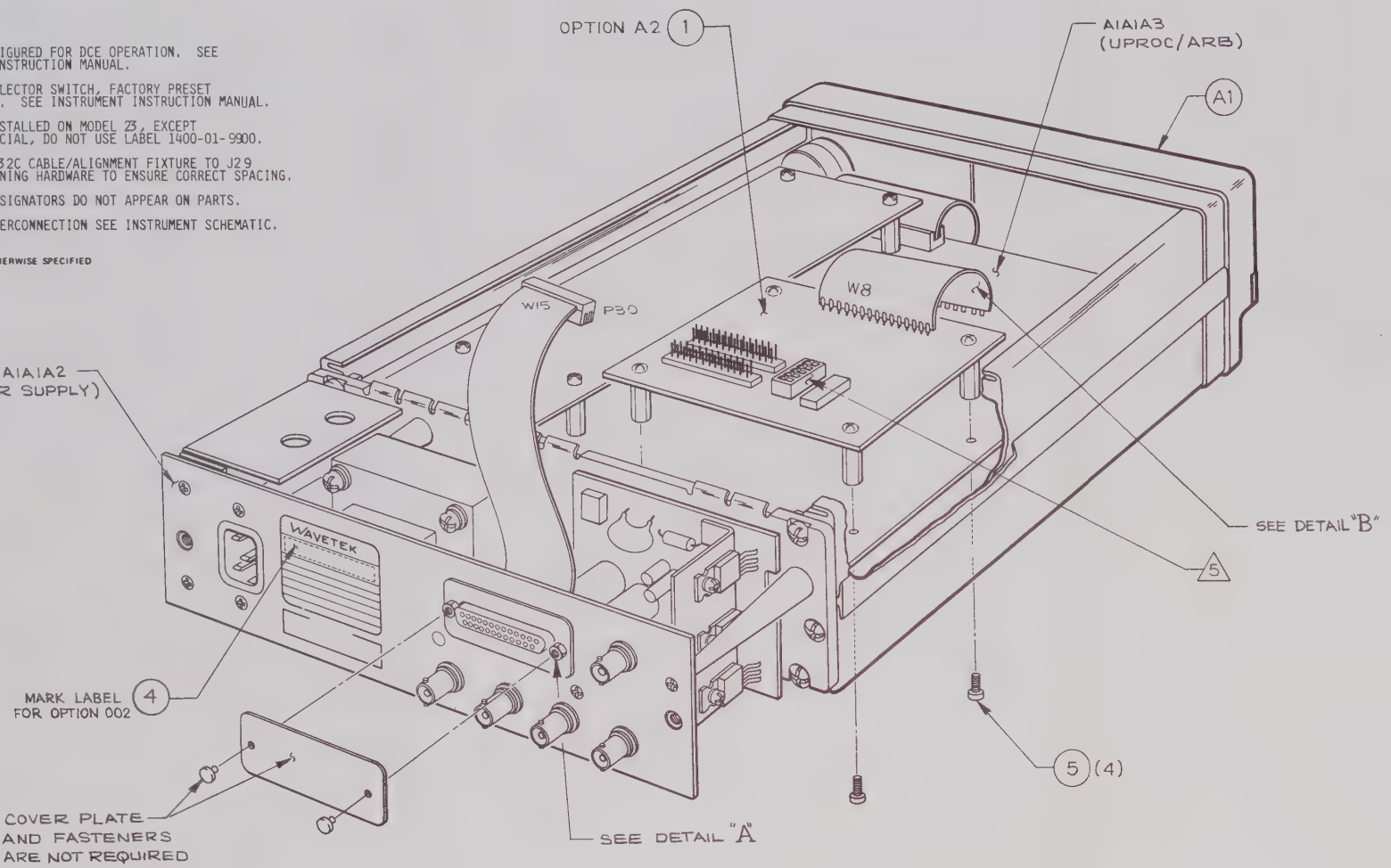
4. IF OPTION INSTALLED ON MODEL 23, EXCEPT MODEL 23 SPECIAL, DO NOT USE LABEL 1400-01-9900.

3. INSTALL RS-232C CABLE/ALIGNMENT FIXTURE TO J29 WHILE TIGHTENING HARDWARE TO ENSURE CORRECT SPACING.

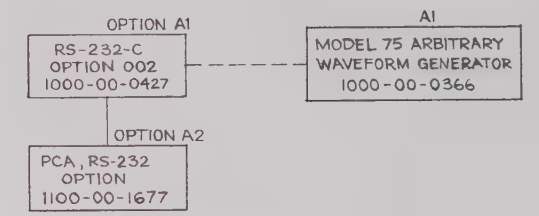
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.

1. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC.

NOTE. UNLESS OTHERWISE SPECIFIED

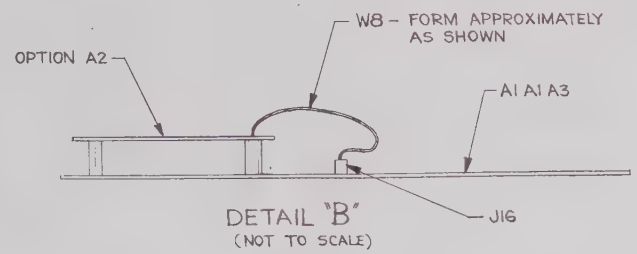


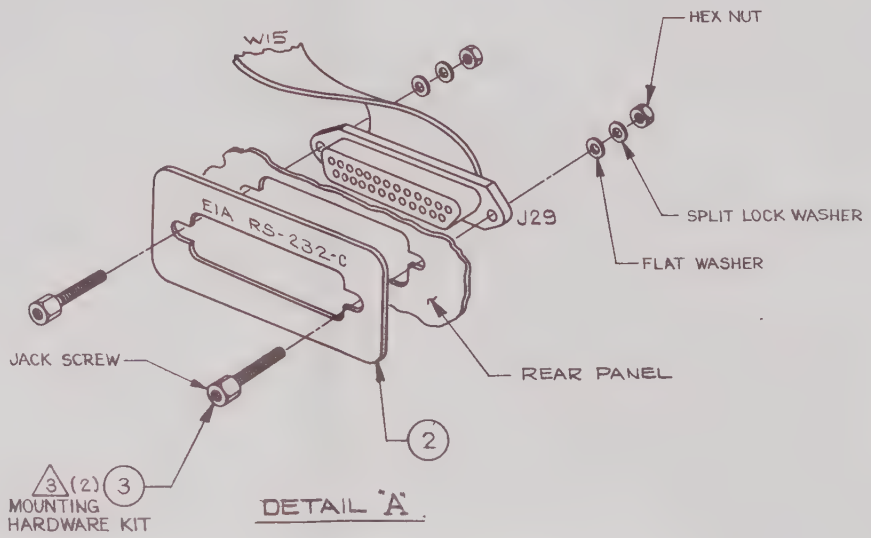
CABLE HOOKUP CHART		
REF DES	DESTINATION FROM	TO
W8	P16	A1A1A3-J16
W15	P30	OPTION A2-J30C (6)



REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ACCEPTANCE TEST SPECIFICATION	23/75-0427	WVTK	0007-00-0427	1
1	PCA, RS-232 OPTION	1100-00-1677	WVTK	1100-00-1677	1
2	PLATE, RS-232 ADAPTER	23/75-9643	WVTK	1400-01-9643	1
3	MODIFICATION, JACK SCREW	23/75-9669	WVTK	1400-01-9669	2
4	LABEL, OPTION, MODEL 75	1400-01-9900	WVTK	1400-01-9900	1
5	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
W15	ASSY, RIBBON CABLE	6002-00-0029	WVTK	6002-00-0029	1

INSTRUMENT COVERS NOT SHOWN





NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 7/3/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJENGR		TITLE: RS-232-C, OPTION 002
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO 23/75
	SCALE NONE		DWG NO 1000-00-0427 REV
	CODE IDENT 23338		SHEET 2 OF 2

1000-00-0427

BISHOP GRAPHICS-ACCUPRESS REORDER NO. A27088

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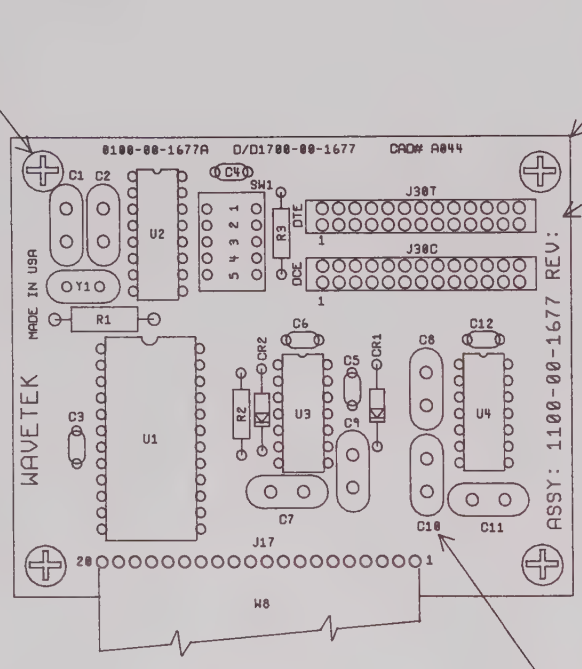
REV	ECN	BY	DATE	APP

(REF) 1
(REF) 3

(4) 1
(4) 3



2

SEE NOTE 4

SEE NOTE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, RS-232 OPTION	0103-00-1677	WVTK	0103-00-1677	1
1	STANDOFF	013-003-2	WVTK	1400-00-2303	4
C12 C3 C4 C5 C6	CAP, CER, MN, .1MF, 50V, Z 5U, +80/-20% RAD LD SP .2	5028E850RD104Z	KYCRA	1500-01-0420	5
C7 C9	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C10 C11 C8	CAP, MICA, 470PF, 500V	DM15-471J	ARCO	1500-14-7100	3
C1 C2	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	2
2	RS-232 OPTION BOARD	1700-00-1677	WVTK	1700-00-1677	1
J30C J30T	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	2
Y1	CRYSTAL, 2.4576 MHZ	VF246	VA-FI	2300-99-0019	1
3	SCREW, SELF LOCKING, PAN HEAD 4-40X3/16	4-40 X 3/16	CMRCL	2800-23-4103	4
R1	RES, C, 1/2W, 5%, 10M	RC-1/2-106J	STKPL	4700-25-1005	1
R2	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R3	RES, MF, 1/8W, 1%, 6.04K	RN55D-6041F	MEPCO	4701-03-6041	1
CR1 CR2	DIODE	1N5282	FAIR	4801-01-5282	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, RS-232 OPTION	1100-00-1677	

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
SW1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
W8	CABLE, FLEXIBLE FLAT 2", 20 PIN	1-88665-9	AMP	6001-60-0008	1
U3	IC, QUAD LINE DRIVER, RS-232C	MC1488	MOT	8000-14-8800	1
U4	IC, QUAD LINE RECEIVER, RS-232C	MC1489L	MOT	8000-14-8900	1
U1	IC, 1.0 MHZ ASYNCH COMM INTERFACE ADAPTER	MC6850	MOT	8000-68-5000	1
U2	IC, CMOS PROG BIT RATE GENERATOR	HD-4702-9	HARIS	8004-70-2900	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, RS-232 OPTION	1100-00-1677	

PAGE 2

4. MARK ASSEMBLY REVISION LETTER IN AREA SHOWN.
3. SEE INSTRUMENT SCHEMATIC FOR ASSEMBLY INTERCONNECTION.
2. SEE 0103-00-1677 FOR CIRCUIT SCHEMATIC.
1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REFERENCE DESIGNATION .

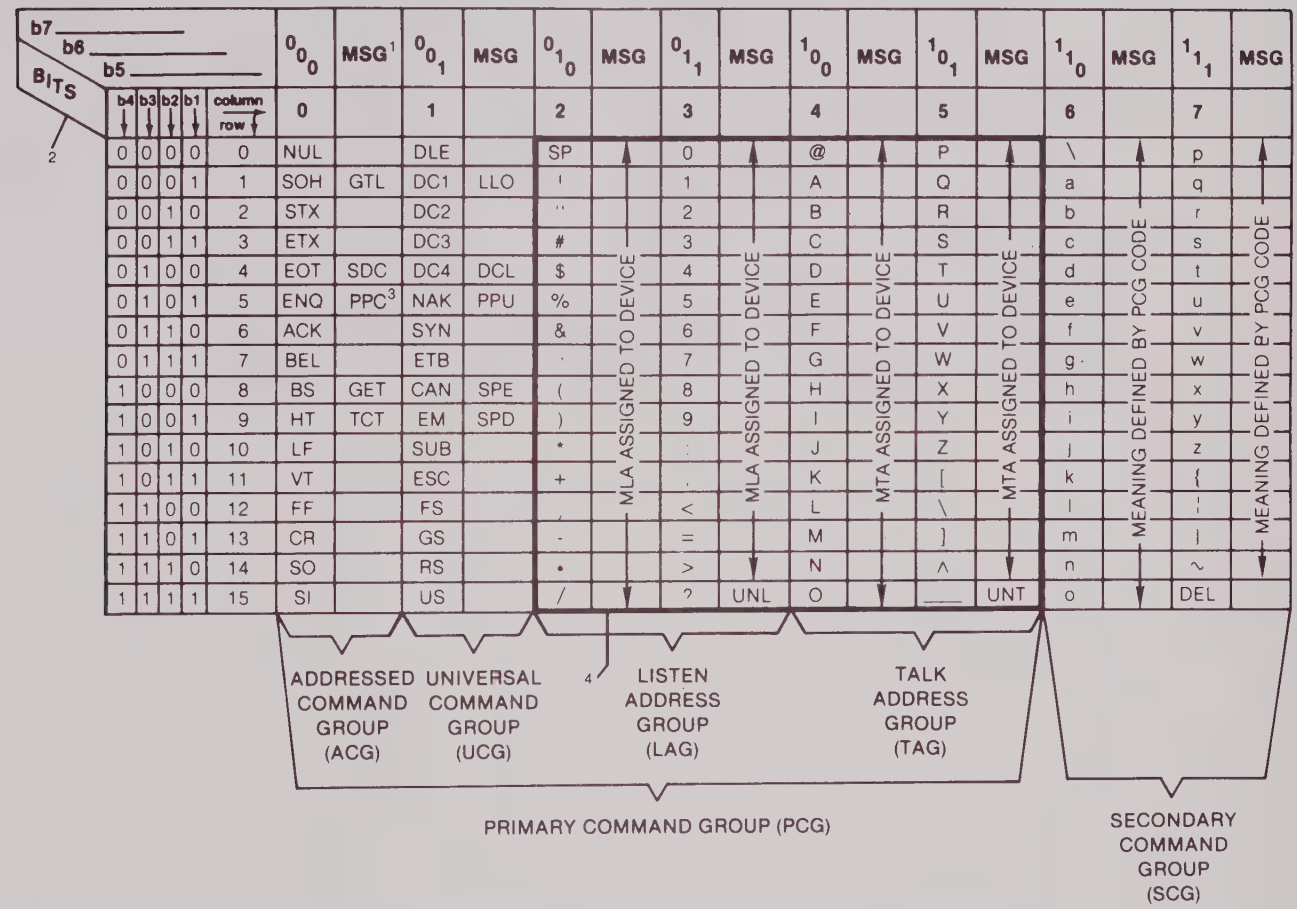
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B. REDMAN	DATE 3/20/85	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE PCA, RS232 OPTION
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 25/75 — DRAWING NO 1100-00-1677 — REV A
	SCALE		CODE IDENT 23338 — SHEET 1 OF 1

1100-00-1677 A

APPENDIX A

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)


b7
b6
b5
BITS
b4 b3 b2 b1 column row
0 0 0 0 0 NUL
0 0 0 1 1 SOH GTL
0 0 1 0 2 STX
0 0 1 1 3 ETX
0 1 0 0 4 EOT SDC
0 1 0 1 5 ENQ PPC3
0 1 1 0 6 ACK
0 1 1 1 7 BEL
1 0 0 0 8 BS GET
1 0 0 1 9 HT TCT
1 0 1 0 10 LF
1 0 1 1 11 VT
1 1 0 0 12 FF
1 1 0 1 13 CR
1 1 1 0 14 SO
1 1 1 1 15 SI
0 0 MSG1
0 1 MSG
1 0 MSG
1 1 MSG
0 1 2 3 4 5 6 7
DLE DC1 LLO
DC2
DC3
DC4 DCL
NAK PPU
SYN
ETB
CAN SPE
EM SPD
SUB
ESC
FS
GS
RS
US
SP ! " # $ % & ' ( ) * + , - . /
0 1 2 3 4 5 6 7 8 9 : ; < = > ?
UNL
@ A B C D E F G H I J K L M N O
P Q R S T U V W X Y Z [\ ] ^ _
UNT
` a b c d e f g h i j k l m n o
p q r s t u v w x y z { | } ~ DEL
MLA ASSIGNED TO DEVICE
MTA ASSIGNED TO DEVICE
MEANING DEFINED BY PCG CODE
ADDRESSED COMMAND GROUP (ACG)
UNIVERSAL COMMAND GROUP (UCG)
LISTEN ADDRESS GROUP (LAG)
TALK ADDRESS GROUP (TAG)
PRIMARY COMMAND GROUP (PCG)
SECONDARY COMMAND GROUP (SCG)

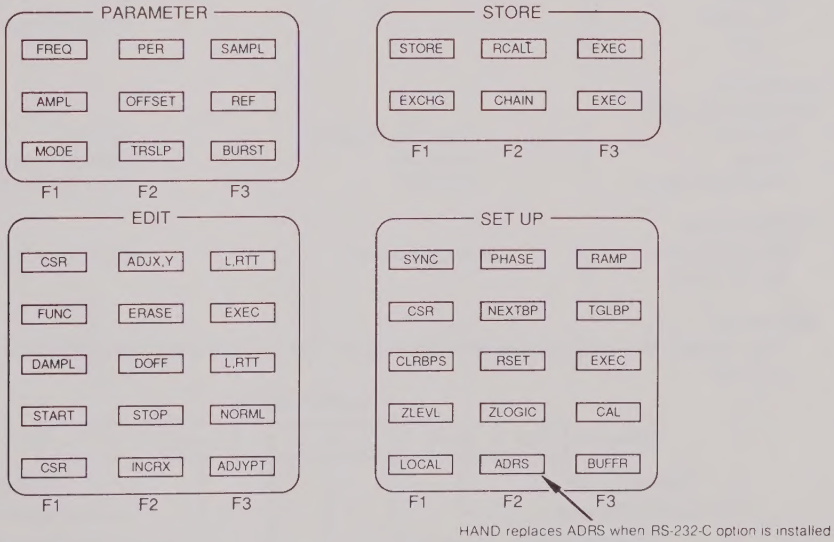
[1]MSG = INTERFACE MESSAGE (FOR THE IEEE-488)
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

MODEL 75 QUICK REFERENCE GUIDE

Soft Key Assignments



***ADdResS**	Digital **AMPL**itude	***†LOCAL**	**ReSET**
ADJust **X, Y** coordinate	Digital **OFF**set	**MODE**	**SAMPL**e frequency
ADJust **Y PoinT**	**ERASE** waveform	**NEXT B**reak **P**oint	**START** address
AMPLitude	**EXEC**ute	**NORMaL**ize waveform	**STOP** address
***†**Command **BUFFeR**	**EXCH**an**G**e waveform	**OFFSET**	**STORE waveform**
BURST count	**FREQ**uency	**PER**iod	**SYNC** address
CALibrate	**FUNC**tion	**PHASE** difference	**ToGgLe Beak Point**
CHAIN	**†HAND**shake mode	**RAMP** time	**TR**igger **SLoPe**
CLea**R** all **B**reak **P**oint**S**	**INCR**ement **X**	**ReCALL waveform**	**Z** axis **LEVeL**
CurSoR	Left, or **R**ight **T**humb **T**ack	**REF**erence	**Z** axis **LOGIC**

*IEEE-488 (GPIB)
†RS-232-C
Communication related softkeys (*, †) only appear when appropriate option is installed.

To Initialize Instrument: Press **Setup** repeatedly until **RSET** is displayed above **F2**. Press **RSET (F2)**, **EXEC (F3)**.

APPENDIX B (Cont)

MODEL 75 REMOTE PROGRAMMING

To Display a Current Setting: Press menu key and soft key for that setting.

To Go To Local: Press **Setup** menu key until **LOCAL** is displayed above **F1**. Press **F1**.

To Recall Commands: Press **Setup** menu key until **BUFFR** is displayed above **F3**. Press **F3** and rotate control knob.

Control Codes

Prefixes (Numerics Follow)

*Sample Freq	F	*Stop Address	P	Arb Data	L
*Amplitude	A	*Sync Address	S	Calibration	N
*Offset	D	*Ramp Rate	M	Set Terminator	XV
*Burst Count	U	Arb Address	K	Set Brk Point	V
*Start Address	T			Clear Brk Point	W

Standard Waveforms

DC	C4	Ramp Up	C3	Cosine	C6
Square	C2	Ramp Down	C5	Inv Sine	C7
Triangle	C1	Sine	C0	Haver Sine	C8

Operation Modes		Trigger Slope		Reference	
*Continuous	B0	*Positive	Q0	*Internal	R0
*Triggered	B1	*Negative	Q1	*External	R1
*Gated	B2				
*Toggled	B3			*Requires execute (I)	
*Burst	B4				

Commands

GPIB and RS-232-C

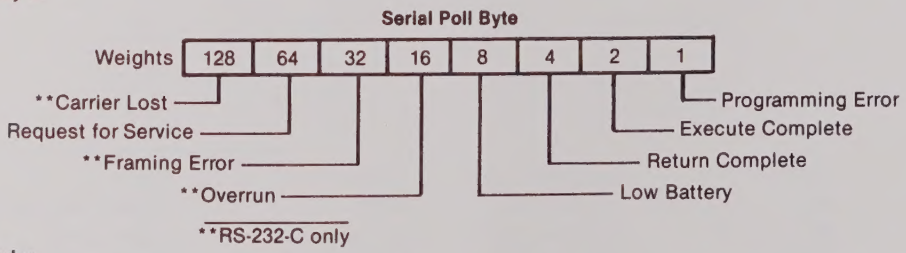
Execute	I	Man Trig Unassert	H	Return	G
Reset	Z	Hold Off	XH0	Display Counter	XC
Man Trig Assert	J	Hold On	XH1	Clear All Break Points	Y

RS-232-C Only

Go To Remote	!	Local Lockout	*	Send Talk Msg	?
Go To Local	$				

SRQ Modes

XQn; Where n is a number representing the sum of the weights of the desired SRQ sources from the serial poll byte.



**RS-232-C only

Talk Modes

XT0	Programming error list.	XT3	Current instrument setup.	XT7	Waveform data at current waveform address, also causes the current address to be incremented.
XT1	Poll byte.	XT4	Pending instrument setup.		
XT2	Most recently selected parameter and its value.	XT5	Instrument and version.		
		XT6	Waveform counter value.		

Other

E	Prefix for exponent in numeric entry.
'Text'	Single or double quote marks designates text to be displayed.

Programming Errors

Talk response when Talk Mode is XT0.

E	No Errors
E1 followed by parameter code	Parameter programmed outside legal limits.
E2AD	Amplitude, offset conflict
E3PST	Start, stop, sync conflict

Initial Power-On Conditions

GPIB Address:	Setting of DIP switch***.
GPIB Terminator:	10 (ASCII line feed)
RS-232-C Terminator:	0 (ASCII CR and LF)
Talk Mode:	0 (Programming error list)
SRQ Mode:	1 (Programming error)

***Located under top cover. Use setup menu and **ADRS** soft key to examine or change the address.

MP MASTER
MA26209